

ENPIRION

Application Note Paralleling Circuit Design with EN5365/66

Introduction

The EN5365 and the EN5366 are 6 A voltage-mode synchronous buck converters operating at a fixed frequency of 5 MHz with internal inductors. The EN5365 offers three-pin VID codes to set the output voltage to one of seven pre-programmed voltages, while the EN5366 offers an adjustable output voltage, set by an external resistor divider. Both devices have a built-in paralleling feature that allows 2 to 4 converters to be paralleled together to increase load current capability up to 24 A. This application note details circuit operation, component selection, performance characteristics and layout considerations to facilitate the design process.

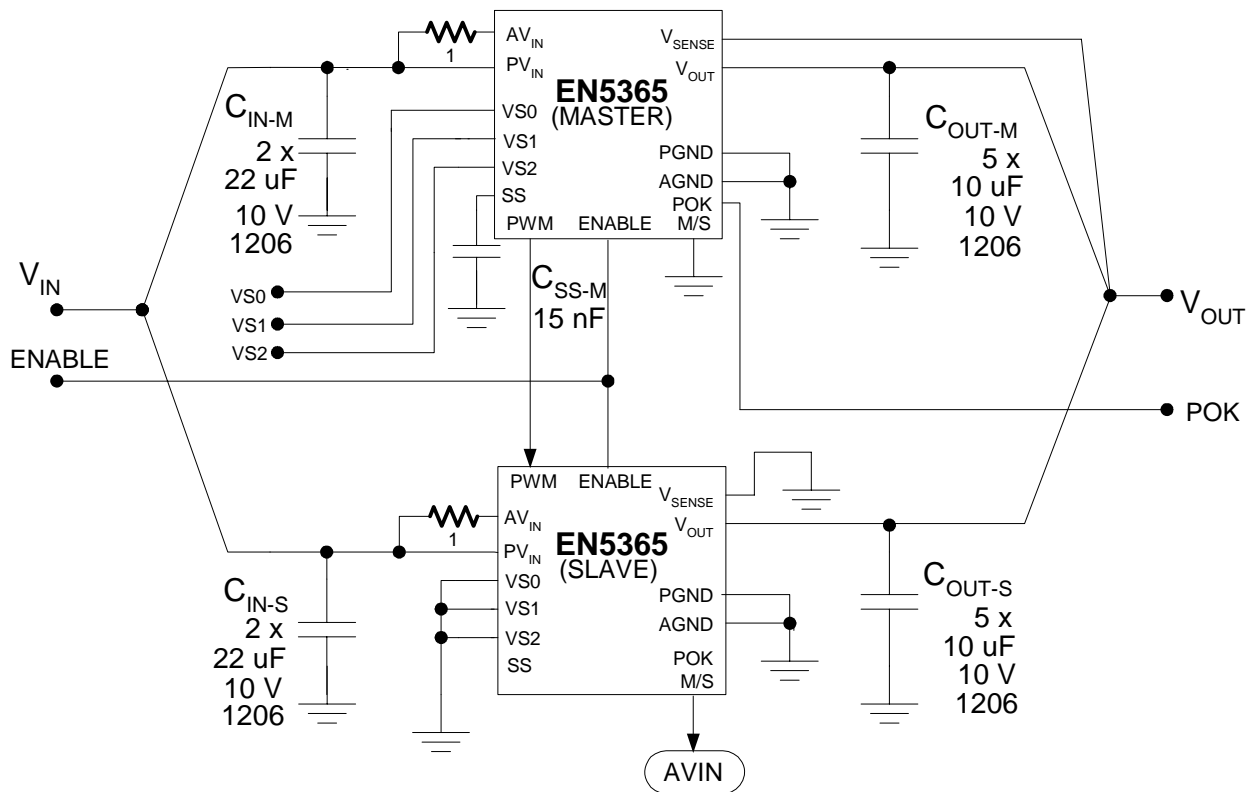


Figure 1. EN5365 Paralleling Circuit

Circuit Operation

Two typical application circuits are shown in Figures 1 and 2 for paralleling two EN5365 and EN5366 devices to deliver 12 A load current. The M/S pin of each device declares which device is Master and which is Slave. Master is the converter with the M/S pin pulled low (to ground). The Master provides the PWM signal to a Slave and synchronizes the turn-on and turn-off of the internal P-channel and N-

channel MOSFETs in both devices. The Master also sets the output voltage through its VID codes (with the EN5365) or its external resistor divider (with the EN5366); the soft-start ramp through its soft-start capacitor and provides the POK signal output.

Slave is the converter with the M/S pin pulled high (to V_{IN}). The Slave provides the power stage and follows the Master. Many internal control functions in a Slave are disabled. As a result, it is recommended to ground the VS0, VS1, VS2, and VSENSE pins and leave the SS and POK pins open in the EN5365 Slave. Likewise, it is recommended that the XFB be grounded and the XOV, SS and POK pins left open in the EN5366 Slave. The POK pin in the Slave will always be low; therefore it must not be connected to the Master's POK.

A $1\ \Omega$ resistor is added between PV_{IN} and AV_{IN} on each device to provide additional filtering of the on-chip supply for stable operation. Please refer to the EN5365 and EN5366 datasheets for details on each converter and device operation.

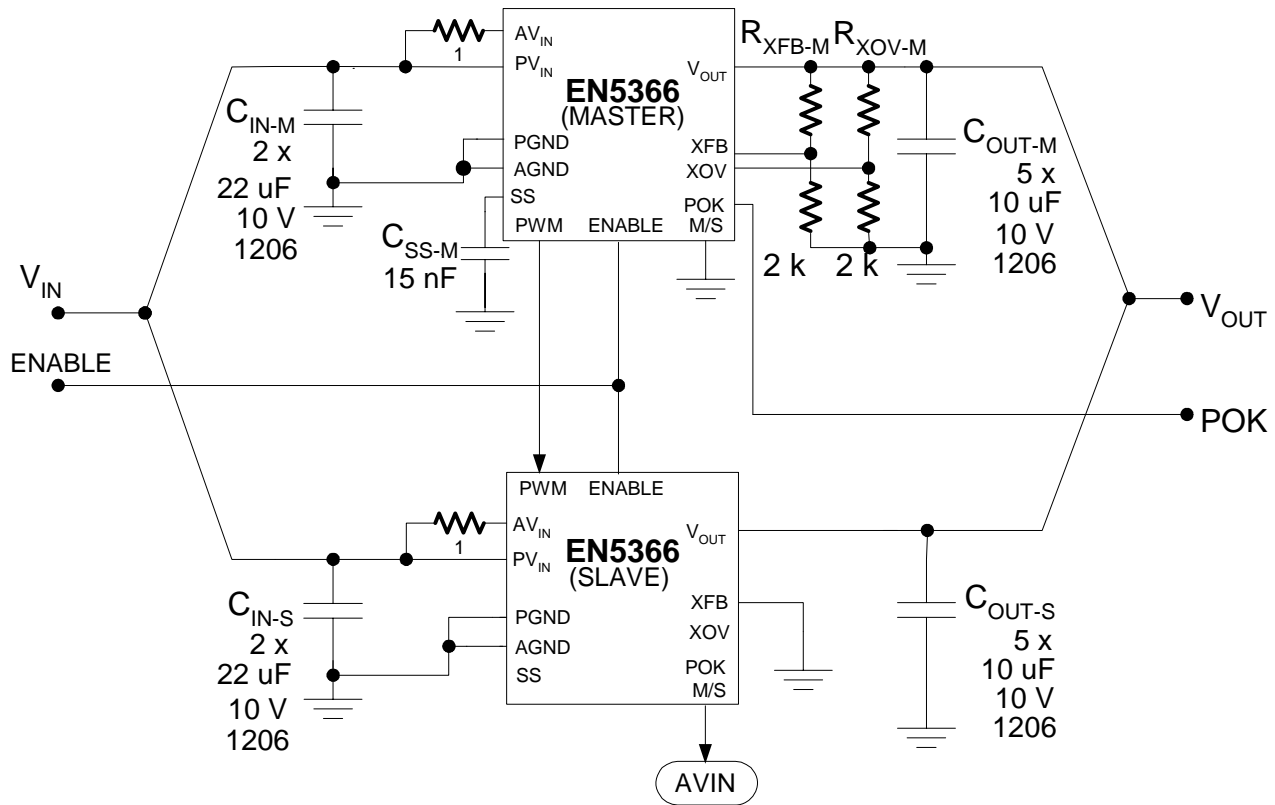


Figure 2. EN5366 Paralleling Circuit

Component Selection

Input and Output Capacitors

The power stage for both Master and Slave should be identical. Two $22\ \mu\text{F}$, $10\ \text{V}$, X5R or X7R ceramic capacitors in 1206 or 1210 packages are recommended on each converter's input in order to provide sufficient ripple current capability and capacitance on the input. Each converter's output can

have five 10 μF , 10 V, X5R or X7R ceramic capacitors in a 1206 package for best ripple performance or a single 47 μF , 10 V, X5R or X7R ceramic capacitor for minimal footprint.

Soft-Start Capacitor

A soft-start capacitor on Master is needed to control the soft-start ramp. This capacitor begins to charge when ENABLE and AVIN cross their turn-on thresholds. The typical soft-start time for the output to reach regulation voltage from when C_{SS} begins to charge is given by:

$$t_{SS} = C_{SS} * 0.075$$

Where the soft-start time t_{SS} is in ms and the soft-start capacitance C_{SS} is in nF. Typically, a capacitor around 15 nF or larger is recommended.

VID Code Setting for EN5365 Paralleling Circuit

Three VID codes VS2, VS1 and VS0 allow the user to obtain one of the seven pre-programmed output voltages. A logic low can be obtained by pulling the pin low (to ground). A logic high can be obtained by pulling the pin high (to V_{IN}). Table 1 shows a matrix of these pre-programmed voltages.

Table 1. Pre-Programmed Output Voltage Setting

VS2	VS1	VS0	Output Voltage
L	L	L	3.3 V
L	L	H	2.5 V
L	H	L	1.8 V
L	H	H	1.5 V
H	L	L	1.25 V
H	L	H	1.2 V
H	H	L	0.8 V

Resistor Dividers for EN5366 Paralleling Circuit

Resistor dividers are only needed on Master, as stated earlier. Use a 2 k Ω resistor for the bottom of both dividers. Then the top resistors R_{XFB_M} and R_{XOV_M} in k Ω can be calculated by:

$$R_{XFB_M} = (V_{OUT} - 0.75) / 0.375$$

$$R_{XOV_M} = (V_{OVTH} - 0.9) / 0.45$$

Where V_{OUT} is the output voltage in V and V_{OVTH} is the desired over-voltage threshold in V. 1% or better resistors are typically recommended for these resistor dividers.

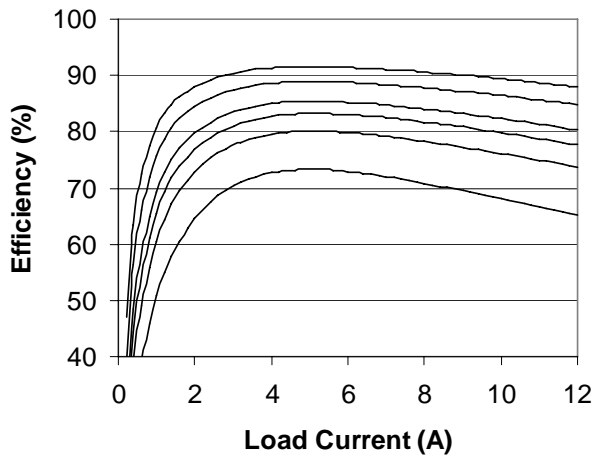


Typical Performance Characteristics

Circuit of Figure 1, $V_{IN} = 5\text{ V}$, $V_{OUT} = 1.2\text{ V}$ and $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted.

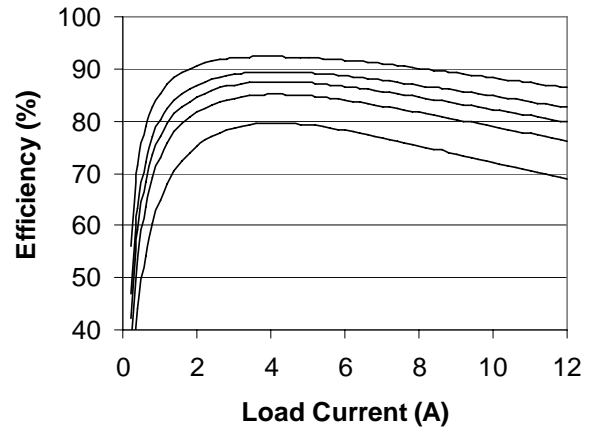
Note: Master/Slave current mismatch ratio is defined as $(|I_{MASTER} - I_{SLAVE}|) / (0.5 * I_{LOAD}) * 100\%$. X_{XX-M} and X_{XX-S} represent the respective Master and Slave voltage or current.

Efficiency vs. Load Current ($V_{in} = 5\text{ V}$)



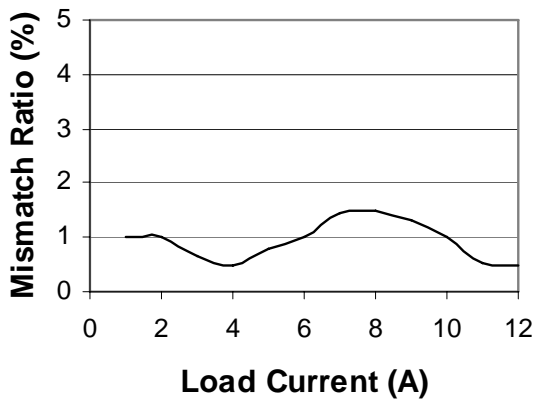
From Top: $V_{OUT} = 3.3\text{ V}, 2.5\text{ V}, 1.8\text{ V}, 1.5\text{ V}, 1.2\text{ V}, 0.8\text{ V}$

Efficiency vs. Load Current ($V_{in} = 3.3\text{ V}$)

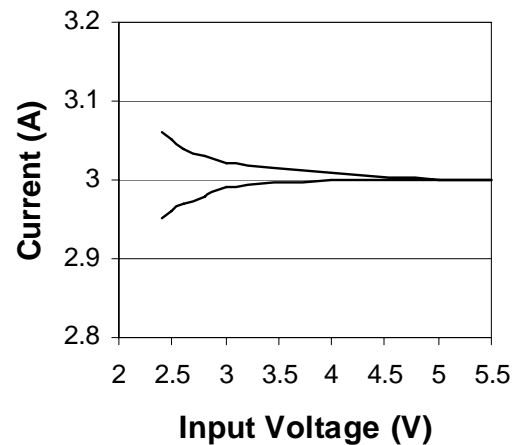


From Top: $V_{OUT} = 2.5\text{ V}, 1.8\text{ V}, 1.5\text{ V}, 1.2\text{ V}, 0.8\text{ V}$

Master/Slave Current Sharing over Load

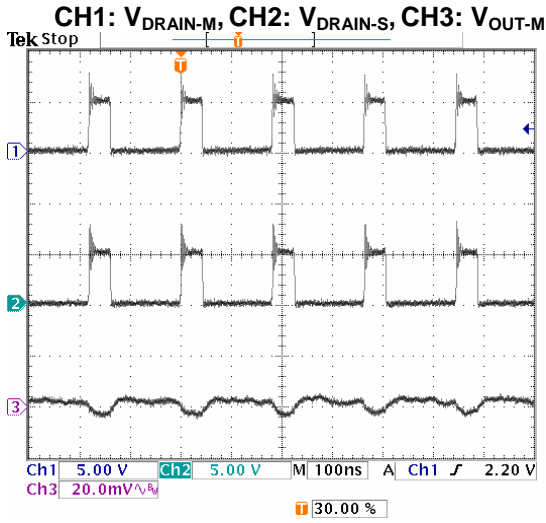


Master/Slave Current Sharing over Line at 6 A Load

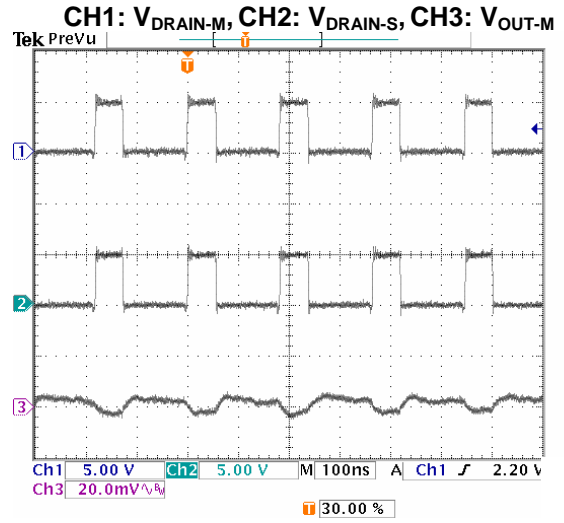


Top: Slave, Bottom: Master

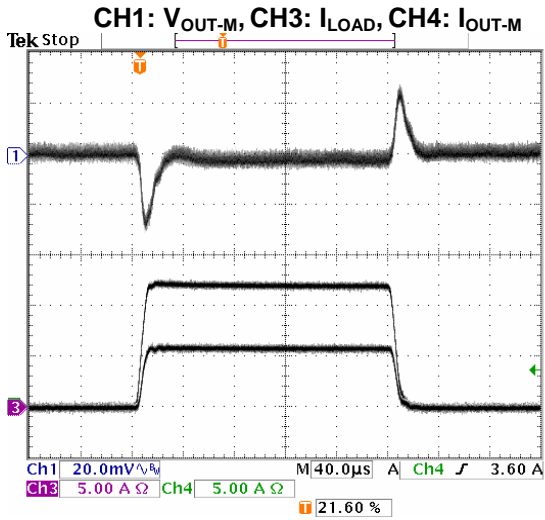
Steady-State Operation at No Load



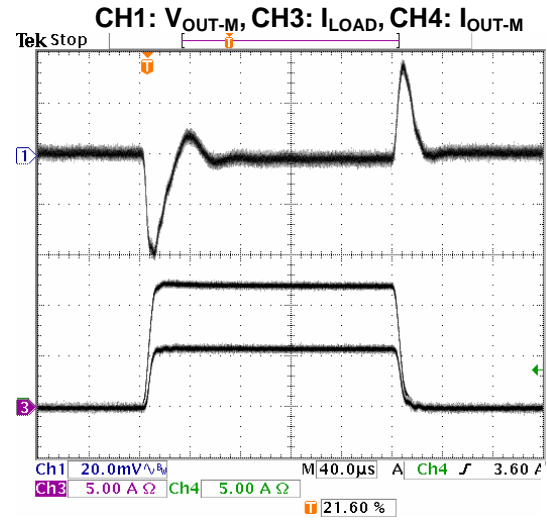
Steady-State Operation at 12 A Load



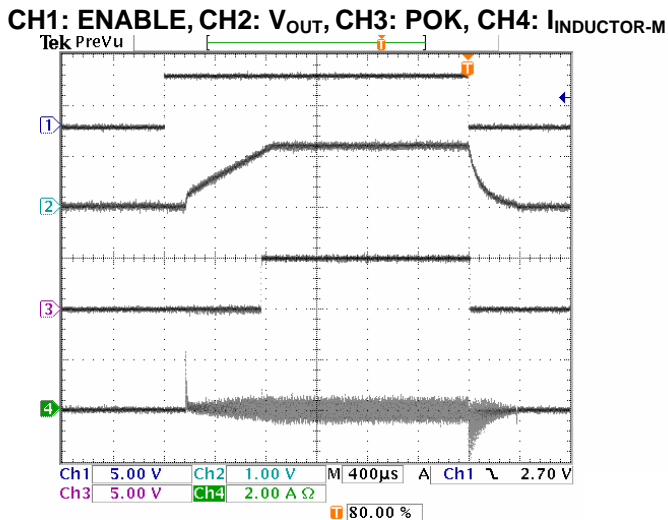
Transient Response at V_{IN} = 5 V (0-12 A Load Step)



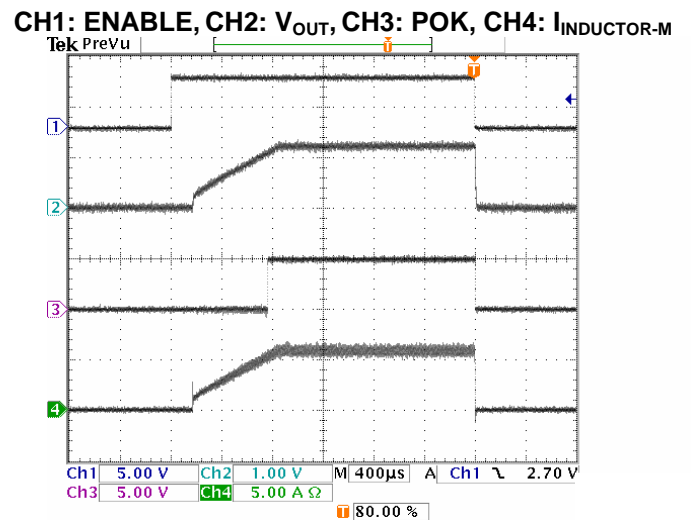
Transient Response at V_{IN} = 3.3 V (0-12 A Load Step)



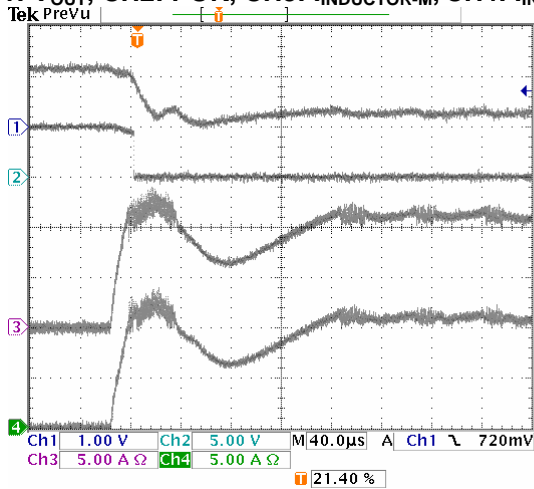
Power-Up/Down at No Load



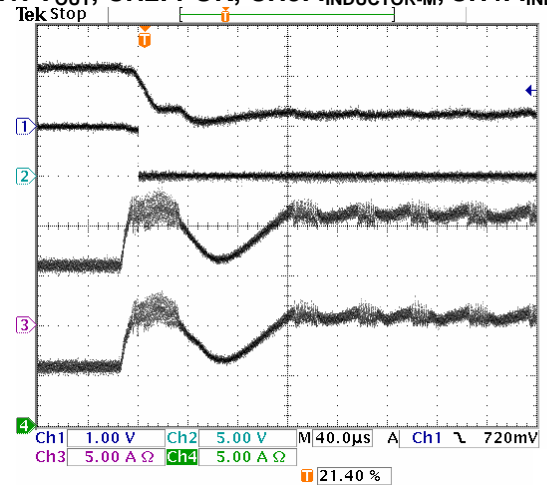
Power-Up/Down at 0.1 Ω Load



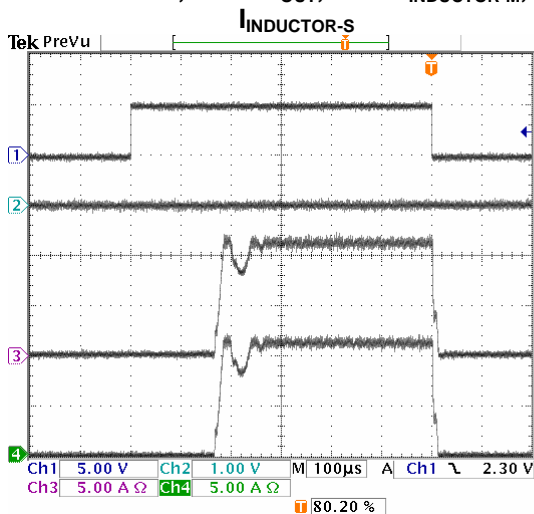
Output Shorted to GND at No Load

CH1: V_{OUT} , CH2: POK, CH3: $I_{INDUCTOR-M}$, CH4: $I_{INDUCTOR-S}$ 

Output Shorted to GND at 12 A Load

CH1: V_{OUT} , CH2: POK, CH3: $I_{INDUCTOR-M}$, CH4: $I_{INDUCTOR-S}$ 

Power-Up/Down with Output Dead Short

CH1: ENABLE, CH2: V_{OUT} , CH3: $I_{INDUCTOR-M}$, CH4:

Layout Considerations

For best current sharing and EMI performance, special attention needs to be paid to layout.

1. Master and Slave should have identical placements with the same values and numbers of input and output capacitors. The input, input GND, output, and output GND of Master and Slave should be connected together via short PCB traces of identical width and length before connected to the system input and output. The output and output GND connection is especially critical and will affect current sharing to a great extent. The maximum resistance difference in PCB traces between the outputs should be less than 10 mΩ. The maximum difference of the input voltage between any two devices should be less than 50 mV. If the paralleling point cannot be equidistant from all converters, the one closest to the paralleling point should be Master.



2. All Master and Slave devices should have their ENABLE pins tied together and should be operated simultaneously with a fast rising edge of 10 μ s or less, to ensure that devices start up at the same time. Startup imbalance could lead to OCP condition in the first device to start up.
3. The PWM pin from the Master device is connected to all Slave device PWM pins. Use short and wide traces to make connections and avoid routing these traces around noisy nodes in the circuit.
4. Master VSENSE pin should be connected to the output for voltage regulation with the EN5365. The VSENSE pin is typically connected to the paralleling point at the output. Likewise, with the EN5366, the XFB resistor divider is typically connected to the same paralleling point at the output.
5. Each individual converter layout should follow the layout guidelines stated in the EN5365 and EN5366 datasheets.

Conclusions

Both the EN5365 and EN5366 work well in paralleling circuits to deliver greater load current. Current sharing is excellent, typically within 2%. Stable operation with internal compensation and minimal component count offers compact solutions for higher current applications.

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