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Chip-level Integration Solves Power Design Issues

Contemporary switch-mode DC-to-DC converters not only occupy significant area on the OEM circuit board, but they are plagued by layout-dependent noise and stability issues. But new breakthroughs in semiconductor processes and magnetic materials have enabled integration of the entire DC-to-DC converter, including ancillary components, into a single IC package. One result is enhanced control over the implementation, allowing converters to be made stable over a very wide range of input/output conditions with no layout dependency issues. Integration of the magnetics makes it possible to dramatically reduce the noise associated with the large pulse currents that pass between the power switches and the inductor. Input/output capacitor loop currents are confined to geometrically small areas thereby reducing noise contributions from that component as well. Full integration reduces noise concerns, reduces part count and footprint, plus speeds design time for this troublesome component.

Troublesome Switchers

The two fundamental choices in voltage regulators are linear and switch-mode. Linear regulators offer simplicity, low part count, good transient performance, and poor efficiency. Switch-mode regulators offer high efficiency, but also high part count, layout sensitivity, noise, and large footprint.

There are many ways to think about how step-down switching power supplies work. In the simplest terms, the power MOSFETs act as switches that “chop” the DC signal up into a pulsed AC wave-form. The pulsed wave is then “filtered” to create a new DC signal. The ratio of the switch on and off times, the duty cycle, determines the new voltage level. A feedback network controls the duty cycle to regulate this output voltage level.

Sounds simple enough. However, there are many sources of trouble. When the switches chop the input they create large pulsed currents that pass through the switch, through the trace interconnect to the output filter. These pulsed currents can create large voltage spikes -- a source of noise. The filter itself is not perfect, and so a significant residual AC “ripple” current and “ripple” voltage remain. The ripple voltage rides on the DC output voltage, creating a noisy supply rail. The ripple current circulates through the switches, the inductor, and the input and output capacitors, acting as loop antennas radiating electrical noise. A further issue is that the switching noise can couple onto the feedback lines and affect regulation or make the regulator unstable altogether. The net effect is that switch-mode converters have the potential to create noise on the circuit board, radiate significant electrical noise, and have poor regulation or even be completely unstable. All of these effects are critically dependent on the layout of the converter components, especially the magnetics.

Making Them Smaller

Integration of Switches, Control, Compensation

The first and most obvious way to reduce the converter footprint is to integrate all components that can be implemented in silicon, including the control and power switches. This requires a semiconductor process that is compatible with both the power MOSFETS and the analog and digital control circuitry.

Lateral Diffuse MOSFETs or LDMOS transistors offer this compatibility. However, so that the devices can tolerate higher input voltages, current LDMOS is restricted to process geometries of 0.5 micron and larger. The consequence is that these devices have relatively high gate capacitances and so have high switching losses. While switching frequencies of 2- 4 MHz are often claimed, these come at a penalty in efficiency.

With LDMOS we can integrate the control, the compensation, the gate drive, and the power MOSFETS. But this is not enough to address the noise and layout issues, nor does it result in a footprint reduction that really makes a difference.

Now What? Ah, the Magnetics!

The magnetics, that is, the inductor, is the source of most of the troubles. The layout and placement of this component is the most important element of the switch-mode DC-to-DC converter design.

The difficulty in converter layout is illustrated in the following discussion. When the power switches open and close, large pulsed currents flow through the switch and into the inductor. This path between the switch and the inductor must have very low impedance or the pulsed current will result in a large voltage “spike”. In a non-integrated converter, the path consists of the wire-bond, the package lead, the lead solder-joint, the board trace, the inductor solder-joint and finally the inductor lead. The total impedance is given as:

$$Z_{TOTAL} = Z_{Wirebond} + Z_{package-lead} + Z_{package-Solder-jo\,\mathrm{int}} + Z_{Trace} + Z_{Inductor-solder-jo\,\mathrm{int}} + Z_{Inductor-lead}$$

The trace and solder joint impedances are the main culprits, having potentially large resistances along with significant reactive components. This leads to noise and ringing from the pulse currents and AC ripple current.

The solution? Bring the inductor inside the package and wire-bond directly from the MOSFETs to the inductor electrode. This eliminates the trace impedance and the solder joints.

Now we have a new category of converter, a turn-key micro-module! The high level of integration yields a foot print reduction of 50 – 80 percent and solves the troublesome noise and layout issues. But, alas, things are never that easy; read on!

But My Inductor and Output Cap are Too Large

Let’s say we are designing a DC-to-DC converter to step down a Lithium Ion battery voltage, nominally 3.6V down to 1.8V. Assume we require a peak sustained current of 500 mA. We want low current ripple, ΔI_{OUT}, so let’s assume that we can allow a ripple of 25% of I_{MAX}. Also assume that our silicon process has good switching loss characteristics at 1 MHz; switching loss is critical for converter efficiency.

The required inductor would be given as:

$$L = \frac{V_{out}\left(1 - \frac{V_{out}}{V_{in}}\right)}{\Delta I_{out} F_{switch}} = \frac{1.8\left(1 - \frac{1.8}{3.6}\right)}{125mA * 1MHz} = 7.2\mu H \approx 10\mu H$$

Since 7.2μH is not a common value, we would chose then next largest catalog value, 10μH. This inductor is too large for integration, especially if shielding is required.

What can be done to make the inductor smaller? We could allow a higher current ripple, but that would lead to more noise and stronger radiated EMI. The answer lies in the inverse dependency on switching frequency. Increasing the switching frequency by a factor of five, to 5MHz, would reduce the needed inductor to a value of 1.4 μH. This value is much more tenable in a very small footprint with low profile; the caveat is that the inductor must be designed for low AC loss at this frequency.

The choice of output capacitor is also inversely proportional to the switching frequency and is given as:

$$C_{out(\min)} = \frac{\Delta I_{out}}{8 \Delta V_{out} F_{switch}}$$

where ΔV_{out} is the maximum allowable ripple voltage. High value output capacitors are both costly and take up significant amounts of board space. Operating at higher switching frequency allows the use of smaller, lower cost capacitors, yielding further footprint reduction.

Switching Loss

Now another problem: you can't just run at a higher switching frequency. For any given semiconductor process, be it power, logic, or analog, there is a switching loss that increases linearly with frequency. The faster you switch, the higher the loss. The equation below describes the relationship:

$$P_{SWITCH-LOSS} = \alpha\left(C_{ISS} + C_{OSS}\right)V^2 f$$

Switching loss results from the charge required to turn the power MOSFETs on and off; to charge and then discharge the input and output capacitances of the transistor.

A common parameter used in the power semiconductor field is known as the "figure of merit"(FOM). This is the product of the gate charge and the MOSFET drain-to-source "on" resistance or $R_{DS(ON)}$, in units of milli-Ohm*nano-Coulombs.

For any given semiconductor process, this FOM is a constant. What that means is that there is always a tradeoff between on resistance, $R_{DS(ON)}$, and switching loss. You can decrease the $R_{DS(ON)}$ and hence reduce the conduction losses in the switch, but the penalty is that switch-loss will increase proportionately. Likewise, you can reduce switching loss, but the conduction loss will then increase; no free lunch.

Semiconductor Process Developments: How to go Faster

The trick, then, is to develop a semiconductor process that has a substantially lower FOM. To achieve this, a base process must be chosen that exhibits very low gate capacitances.

To get to the very low FOM target, we must move to a deep sub-micron CMOS process; one that can tolerate higher voltages. As part of the Power Semiconductor Research Team at Bell Labs, Enpirion engineers tackled this problem with amazing results. While the typical FOM for a power semiconductor device, including LDMOS, ranges from 80-400 mΩ*nC, Enpirion's LDMSO exhibits a FOM that is below 10 mΩ*nC. Since the gate capacitance is reduced by as much as a factor of ten, the device can be operated at ten times the speed for the same efficiency, and use an inductor one tenth the size; viola!

High Frequency Magnetics

Magnetic materials also have a loss component that is frequency-dependent. Operating at high frequencies translates to higher core losses. It is not enough to move to higher frequencies to get to a smaller inductor value; it is critical to address this AC loss component as well.

Conventional magnetics overcome AC core loss by increasing core volume; that is, making the inductor larger. Not the direction we are trying to go.

Enpirion has developed a family of MEMS-based (Micro Electro Mechanical Systems) inductors that are fabricated in a CMOS manufacturing process flow compatible environment that will ultimately lead to monolithic integration of silicon and magnetics.

The culprit in AC core loss is eddy current. The common way to deal with eddy current is to restrict the path over which it can flow. In transformer design, this is done by slicing the core into thin layers and placing an insulting laminate layer between the slices. With inductors, the approach has been to turn the core material into a powder and form them into ceramics. Then the conduction path is confined to an area the size of a grain of the material. Enpirion's approach has been to take a magnetic alloy, a metal, and disrupt the lattice structure to form an amorphous crystalline solid. Now the eddy current path is restricted to an area the size of a few tens of molecules. This provides excellent high frequency performance.

The result is a high value inductor with small footprint, and most importantly for integration, it has a very low profile.

Practical Applications

Through the course of this article we have discussed the many difficulties associated with switch-mode DC-TO-DC converters. They are very sensitive to layout, have typically high part counts, are potentially a source of unacceptable levels of noise, and they take up a lot of area on the circuit board.

We have shown how integration of the silicon components, and the magnetics, can solve these problems. It is integrating the magnetics that leads to the breakthrough in converter design. Noisy signals are confined inside the package and design is no longer plagued by layout difficulties. External components are reduced to two low-cost ceramic capacitors.

Enpirion has introduced a family of DC-to-DC converter modules in a tiny 4mm x 5mm x 1.1mm QFN package. Using small MLCC capacitors yields a footprint as small as 28mm^2. This is about half to one-fourth the footprint normally required and does not compromise on performance or efficiency.

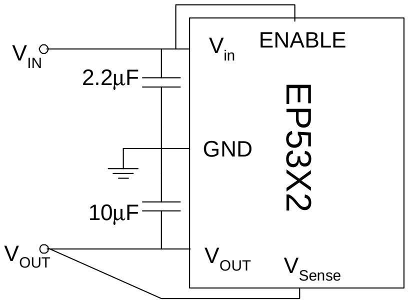

Figure 1. Enpirion EP53x2 800/600/500 mA DCDC

The developments described in this article present an alternative to the dilemma of efficiency versus footprint. Further, the module approach addresses the noise and layout sensitivity problems as well as reducing part count. Problem solved!