



High Frequency Implications for Switch-mode DC-DC Converter Design

by

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Introduction

Traditionally, power engineers are trained to think in the “time-domain” while RF engineers are trained to think in the “frequency-domain”. To successfully design high-frequency DC-DC converters, the engineer will need to jump back and forth freely between the two perspectives. High frequency design requires new attention placed on parasitic impedances, effects from PCB layout, and potential sources of large output ripple switching spikes, and radiated and conducted electrical noise. As switching frequency continue to increase in the drive to reduce power supply footprint, power engineers and system designers will be increasingly faced with issues that are outside of their realm of expertise. This article will help shed some light on the high frequency design considerations when designing with the next generation of fast switch-mode DC-DC converters.

High Frequency Content, It’s Not Just the Fundamental

The trend towards smaller DC-DC converter footprint is driving the industry to ever higher switching frequencies. To understand the impact of high switching frequency on DC-DC converter design, it will be useful to examine the spectral content of the switching waveform. Using the principle of superposition, the switching waveform (fig 1 (a)) can be decomposed into three unique waveforms: a somewhat ideal square-wave (fig 1 (b)), a triangular wave that represents the non-ideal rising edge of the pulse (fig 1 (c)), and a triangle wave that represents the falling edge of the switching waveform (fig 1 (d)). The rectangular waveform is the primary contributor of energy at the fundamental of the switching frequency with the familiar $\sin(x)/x$, or $\text{sinc}(x)$ envelope. The fast rising and falling edges contribute energy at $1/\tau_R$ Hz and $1/\tau_F$ Hz.

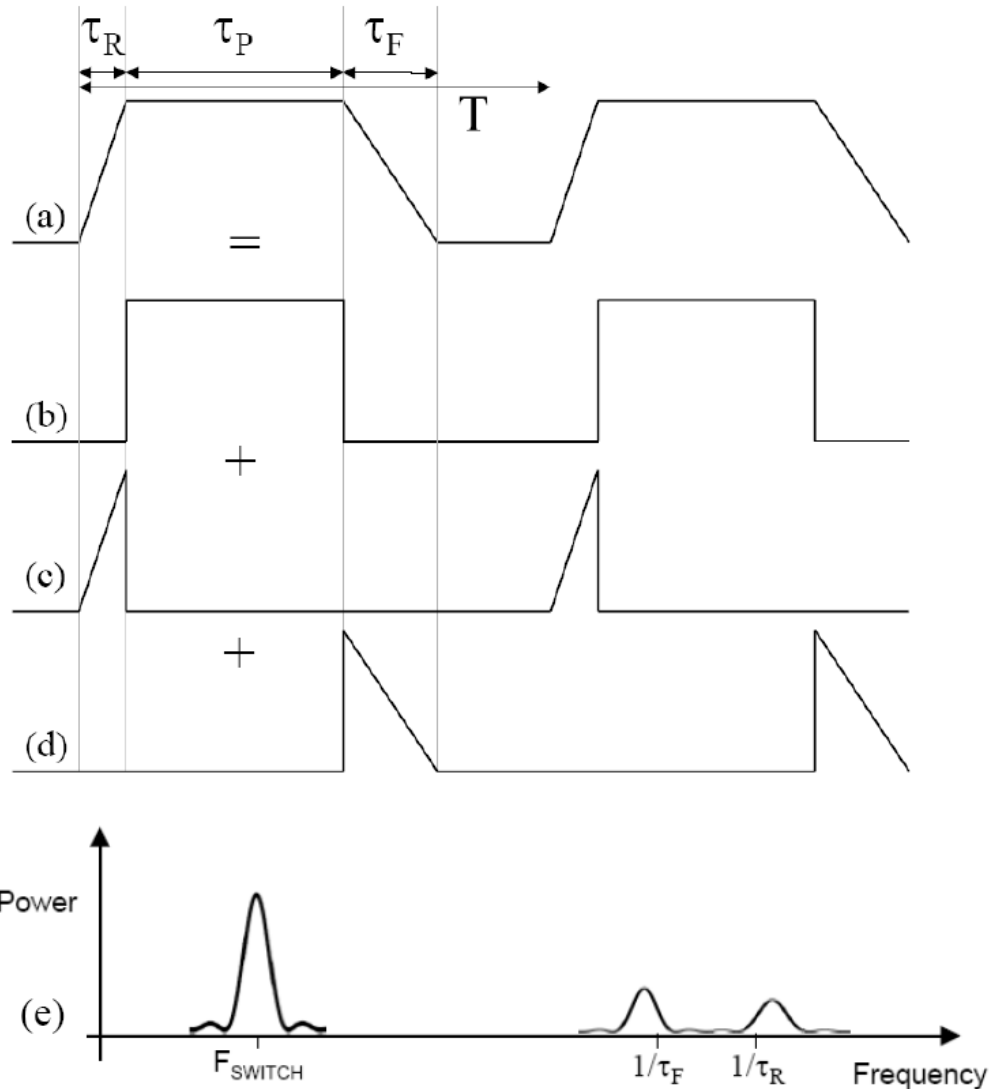


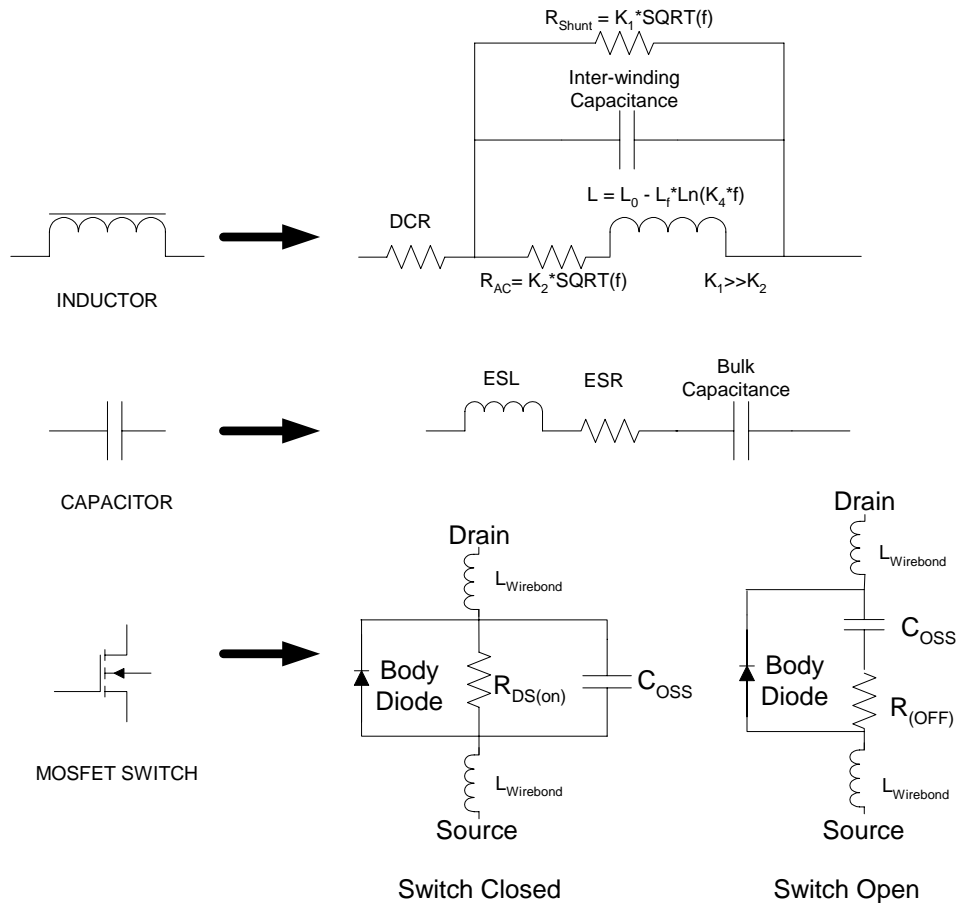
Figure 1. Switching waveform decomposition and associated frequency spectrum.

As an example, the Enpirion, EN5335QI 3A-Integrated Inductor DC-DC converter, operates at a nominal 5 MHz. A 5 MHz switcher will have a 200nS switching period. Good efficiency requires that the rise and fall times be very small relative to the overall switching period. For this particular part, the rise time is 2nS and the fall time is ~ 3 nS. The 2nS rise time corresponds to a frequency contribution at 500 MHz and the 3nS fall-time corresponds to frequency content at 330 MHz. Figure 1 (e) shows the power spectral density.

By considering the switching waveform and its corresponding frequency components, we can better understand the nature of the noise that must be controlled.

High Frequency Device Modeling or When a Capacitor is an Inductor

Now that we have looked at the frequency content of the fast switching waveforms, we now need to consider how our DC-DC converter components behave at these higher frequencies. Figure 2 shows the common elements that make up the DC-DC converter along with their high frequency equivalent circuits.



DEVICE

HIGH FREQUENCY EQUIVALENT

Figure 2. Converter components and their high frequency equivalents.

INDUCTOR

The inductor is a particularly troublesome component. Its high frequency equivalent circuit consists of several frequency *dependent* elements, including the inductance, inductor series AC resistance, as well as a parallel AC resistance. In parallel with the inductance is a small capacitor that represents the inter-winding capacitance.

The parallel LC combination will exhibit an impedance maxima at its self resonant frequency: $f_R = \frac{1}{2\pi\sqrt{L(f)C}}$. Below resonance the inductor will behave as an inductor with increasing loss with increasing frequency. Above resonance, the inductor will behave as a capacitor, with decreasing loss at increasing frequency. Self resonance can occur at a few hundred MHz for higher value inductors or can occur at a few GHz for smaller valued inductors.

Below self-resonance, the inductor will behave as a low-pass filter, but above self-resonance, the inductor will behave as a high-pass filter.

CAPACITOR

The small signal equivalent of the capacitor consists of a series combination of the effective series inductance (ESL), the effective series resistance ESR, and the bulk capacitance. This combination will have a resonance given by:

$f_R = \frac{1}{2\pi\sqrt{LC}}$ where an impedance minima will occur. Below resonance it will behave as a capacitor, with a negative frequency dependent slope. Above resonance, it will have a positive impedance slope and will behave as an inductor.

The ESR and ESL of a MLC capacitor will be dependent among other things, on the case size. For example, a 1206 10uF X5R MLCC will have an ESL of approximately 1-2nH whereas an 0805 10uF X5R MLCC will have an ESL of around 0.5nH. ESR will tend to increase with decreasing case size while ESL will tend to decrease with increasing case size.

MOSFET

The MOSFET, either P-channel or N-channel will have an equivalent circuit that depends on whether the device is turned on, i.e. the switch is closed, or the device is off (switch is open). When the device is on, the equivalent circuit consists of a parallel combination of the $R_{DS(ON)}$, the equivalent output capacitance, or C_{OSS} ($C_{OSS} = C_{gs} + C_{gd}$), and the body diode. When the switch is open R_{DS} becomes very large and so is not part of the equivalent circuit. Instead the equivalent circuit consists of the C_{OSS} in series with its AC ESR. The body diode is modeled as a ideal diode, and becomes important if the DC bias of the junction turns the diode on and offers an alternative conduction path. In series with these will be the wire-bond inductance.

How About the PCB?

At high frequencies, 100MHz to 500MHz, even small parasitic effects become significant. Most of the basic features of a PCB have an associated inductance and distributed capacitance. At high frequencies, inductance is the enemy!

THE TRACE:

If we consider a trace of width W , length ℓ and thickness T , the parasitic inductance can be approximated using Grover's equation for a rectangular conductor:

$$L_{trace} = 0.2 * \ell \left[\ln\left(\frac{2\ell}{W+T}\right) - 0.2235\left(\frac{W+T}{\ell}\right) + 0.5 \right] nH \text{ (dimensions in mm)}$$

The thickness of one ounce copper plating is 0.035mm. Since the calculation always combines the terms of width and thickness, the trace width and length tend to dominate. For a trace of $\ell=10\text{mm}$, $W=1\text{mm}$, $T=0.035\text{mm}$, the resultant parasitic inductance would be about 7nH, quite a significant number when looking at 300-500MHz phenomenon!

THE VIA:

The inductance of a via with outer diameter D_1 plating thickness T , and length ℓ is given by Grover's equation for the inductance of a cylindrical tube:

$$L_{via} = 0.02 * \ell * \left[\ln\left(\frac{4*\ell}{D_1}\right) + G\left(\frac{D_2}{D_1}\right) - 1 \right] nH \text{ (dimensions in mm)}$$

Where:

$D_2 = D_1 - 2 * T$, and
 $G(D_2/D_1)$ is found from table 1.

As an example, consider a PCB with overall thickness of 0.62mm \cong 1.5mm. Then a via with a finished diameter of 0.5mm, from the top layer to the bottom layer, assuming 1 oz. copper plating having thickness 0.035mm, would have an associated inductance of 0.5nH. This may seem small, but it will have a significant effect at higher frequencies.

SKIN EFFECT:

Skin effect refers to the tendency of AC current to flow on the surface of a conductor. The depth of penetration, or skin depth (δ), of an AC current is defined as the point at which the amplitude is attenuated by 1/e (e = base of the natural logarithm) of its surface value:

$$\delta = \sqrt{\frac{\rho}{\pi * \mu * f}} \text{ (meters)}$$

Where:

ρ is the material resistivity,

Table 1.

D2/D1	G(D2/D1)
0.00	0.2500
0.05	0.2488
0.10	0.2452
0.15	0.2395
0.20	0.2320
0.25	0.2228
0.30	0.2123
0.35	0.2007
0.40	0.1880
0.45	0.1745
0.50	0.1603
0.55	0.1456
0.60	0.1304
0.65	0.1148
0.70	0.0989
0.75	0.0827
0.80	0.0663
0.85	0.0499
0.90	0.0333
0.95	0.0167
1.00	0.0000

μ is the material permeability,
 f is the frequency of interest.

The skin depth for copper at 300MHz is about 4 microns and at 500MHz is about 3 microns.

What this means for the designer of the power supply is that the high frequency AC currents will tend to flow over the surface of features and not necessarily through them. As an example, consider a DC-DC filter capacitor on a PCB with 1 ounce copper plating. The thickness of the plating is 0.035mm or 35u (microns). The skin depth at 500MHz is only 3u. One would expect that the AC current would flow through the capacitor then through the pad and down through the via. Because of the skin effect, this is not how the high-frequency AC current will flow. Instead, it will flow over the surface of the capacitor electrodes, then around the outer edges of the pad and then down the outer surface of the via, to the ground plane, following the path of lowest impedance. The parasitic inductance encountered by the AC current will be the inductance of the via, and the inductance associated with the electrically long path around the surface of the pad. Figure 3 illustrates this phenomenon.

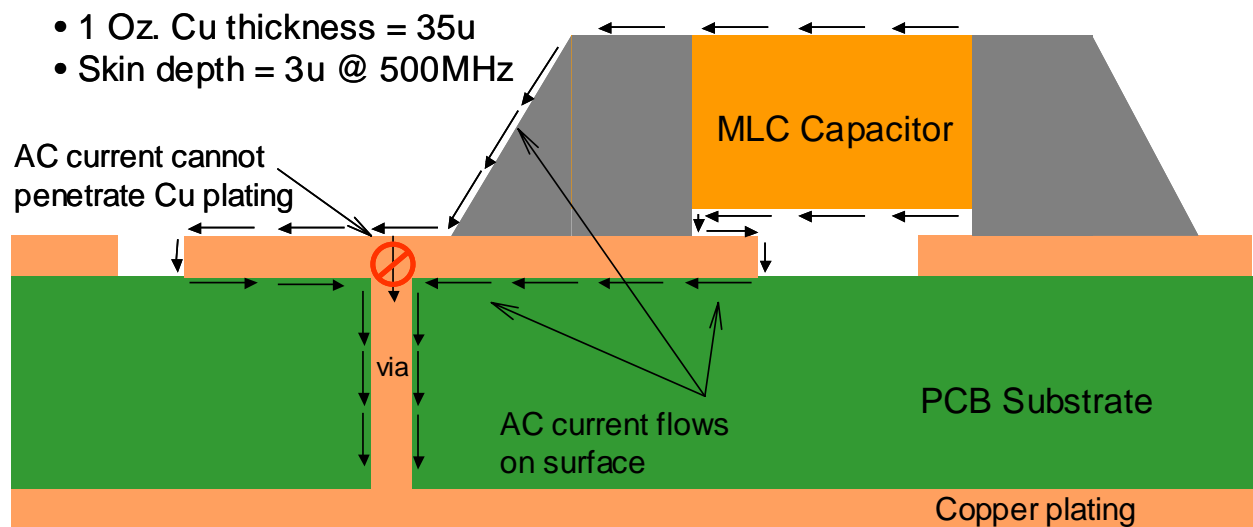


Figure 3. Skin effect and AC current flow on a PCB.

Assembling The Various Parts

We have presented the small signal models for the various DC-DC converter components and shown how to calculate the parasitic elements of the PCB. In this section, we put the various pieces together to come up with a composite high-frequency model of the DC-DC converter and to look at how these affect the performance of the converter.

Probably the simplest converter topology to consider is the “buck” mode, or step-down converter. Figure 4(A) shows the familiar low frequency, or DC, model of a buck converter. The topology uses a P-FET as the high-side switch and a N-FET for the low-side switch. Looking at figure 4(B) we see the high frequency equivalent of the converter itself, but not the parasitic effects of PCB pads, traces, vias, and planes. For convenience the model shows the high-side switch closed and the low-side switch open. Figure 4(C) shows what happens when we include the parasitics from the PCB. Here, we have not only the small signal elements of the components themselves, and the intra-package parasitics from the wire-bonds, but we have also the inductance of the traces, pads, vias, and the ground plane.

Depending on the characteristics of the output filter inductor, it may or may not be operating above resonance. If the high-frequency content is above the resonant frequency, the capacitive element will dominate, and will freely pass the high frequency content. If the high frequency components fall below the inductor self resonance, the impedance will look inductive. The input and output filter capacitors will have a resonance of between 1 and 10 MHz, and so from a high frequency perspective, will be dominated by the inductive properties of the capacitor itself, and of the trace, pad, and via inductances.

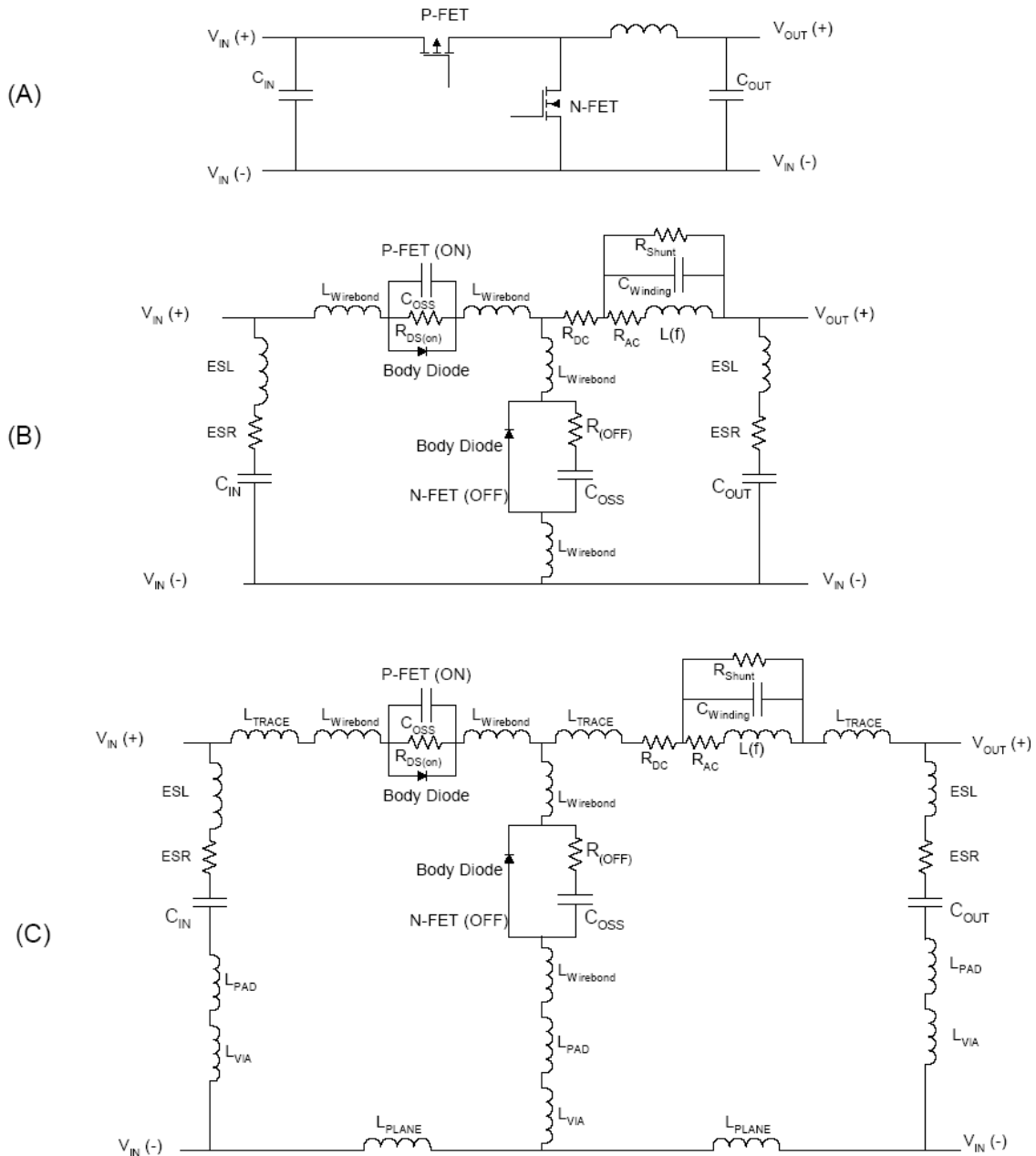


Figure 4. Block diagrams showing, (A) the standard buck topology low frequency model, (B) the high frequency equivalent (N-FET off) absent the parasitic properties of the PCB, and (C) the complete high frequency model including the PCB effects.

High Frequency Performance Considerations

Now that we have put together most of the pieces we can begin to look at HF design issues. These include output ripple voltage, conducted electrical noise, and radiated electrical noise.

Using loop current analysis, we can isolate the input and output current loops as shown in figure 5. The current flowing in the input loop will be a large pulsed current as shown in figure1, while the current in the output loop will be the inductor ripple current plus any coupling from the input loop due to mutual inductances in the current paths.

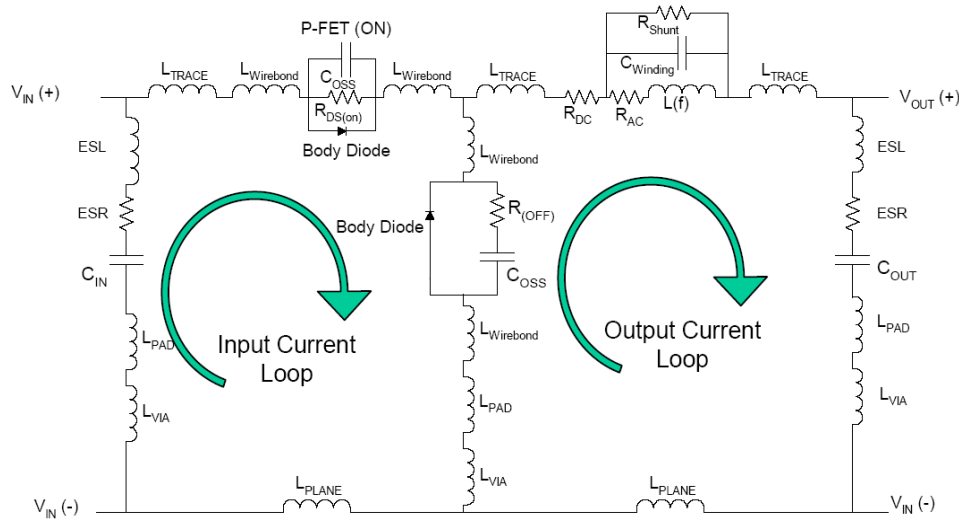


Figure 5. Input and output loop currents.

OUTPUT RIPPLE VOLTAGE:

The output ripple are the AC electrical noise components that make it past the output filter section of the DC-DC converter; that is, the inductor and the output filter capacitor. The ripple voltage is created by the inductor AC ripple current flowing through the output filter capacitor impedance, AND the high frequency components of the input current loop that couple into the output AC current loop through the parasitic mutual inductance in the common portions of the two current loops.

A common mistake that many engineers make is that when they look at the output ripple on their oscilloscope, the scope bandwidth is set to 20 MHz. This is also the typical bandwidth that the DC-DC converter manufacturer shows in their datasheets. Instead, open up the scope bandwidth to the maximum supported by the scope. Make sure and measure the ripple right at the output filter capacitor, using a high impedance probe. This way, you will see the high frequency content in the ripple. If you see switching spikes, try the following:

- The output filter capacitor must have low ESL; less than 1nH is recommended. If necessary, place another lower value ceramic capacitor in parallel with the bulk output filter capacitor.
- Use separate ground pads/plane for the input and output capacitors. This will reduce the mutual inductance between the loop paths.

RADIATED ELECTRICAL NOISE:

The primary source of radiated electrical noise is current flow in the input loop filter but can also be made worse if there is coupling of high frequency noise into the output loop. If you recall from your college electro-magnetics course that currents flowing in a closed path, i.e. a loop act as an efficient radiator of electro-magnetic energy. Maximum radiation efficiency occurs when the loop dimension is on the order of $\frac{1}{2}$ wavelength. To minimize the radiation efficiency, that is to reduce radiated noise, we make the loop as physically small as possible.

- ❑ Input filter capacitor should be placed as close to the DC-DC converter package as possible.
- ❑ Careful attention should be paid to the output filter section as well. An integrated inductor DC-DC converter will help minimize the loop dimension and provide excellent isolation between input and output AC current loops.
- ❑ Be mindful of parasitic inductances in the board traces, solder joints, and component pads. Do not use thermal reliefs in the capacitor pads. High impedances in the primary or intended loop paths may send the currents out onto the PCB, following much larger physical paths and coupling into other circuits. Remember that high-frequency currents follow the path of least impedance, not least resistance!

CONDUCTED ELECTRICAL NOISE:

Conducted electrical noise derives from either stray high frequency currents that act directly on other circuits on the PCB, or from high-frequency AC voltage drops that occur across the various impedances in the intended current path, inductively or capacitively coupling onto adjacent signal or power traces. Either way, the solution is the same. And, coincidentally, are the same for minimizing ripple and radiated noise.

- ❑ Minimize the impedances in the input and output current loops. This ensures that the high frequency currents are confined to these sections and not getting out onto your PCB. Integrated inductor devices help with the impedances between the switching node and the inductor electrode.
- ❑ Minimize current loop path lengths; Integrated inductor enables the smallest possible loop dimensions.
- ❑ Minimize parasitic mutual inductances between the input and output loop

Things to Remember From This Article

- ❑ The switch-mode DC-DC designer must learn to think in both the time and frequency domains.
- ❑ DC current follows the path of least resistance; AC current follows the path of least impedance.
- ❑ At high frequency, a capacitor may “look” like an inductor, and an inductor may “look” like a capacitor.

- Stray inductance is the enemy.

Conclusions

The new generation of switch-mode DC-DC converters will operate at increasingly higher frequencies. High frequency content from these fast switchers leads the power engineer into the realm of RF. Careful attention to the small signal properties of the converter components and the parasitic elements of the PCB will go a long way towards taming the high-frequency beast.