

# Fully Integrated DC-DC Converters

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Dramatic improvements in the rise- and fall-time characteristics of power MOSFETs enable PWM switching frequencies to increase by an order of magnitude. The resulting drop in required inductance permits co-packaging of the inductor and the power-supply controller.

In the not-so-distant past, virtually every component of a power supply was a discrete unit—from the controller IC to the MOSFETs and everything around it. It was difficult and time-consuming just to lay out the board, and any changes in the design created headaches during redesign. In addition, designers had to worry about coupling the controller to the gate drive, which also had to be custom-designed, as well as the magnetics. The next phase of power-supply design saw the

integration of the controller, gate drive and MOSFET in a single silicon chip, which was far simpler. However, one still had to interface this chip to an outside inductor, which historically has been too large to integrate.

Inductor size is a function of operating frequency. Clearly, the key to creating inductors small enough to integrate on a chip is to increase the switching frequency of the converter. Through

recent proprietary innovations in MOSFET design, dramatic improvements in rise- and fall-time characteristics have enabled switching-frequency increases of an order of magnitude over what is available today. The resulting drop

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in required inductance and component size provides a design breakthrough that enables the inductor to be fully incorporated into the power-supply package.

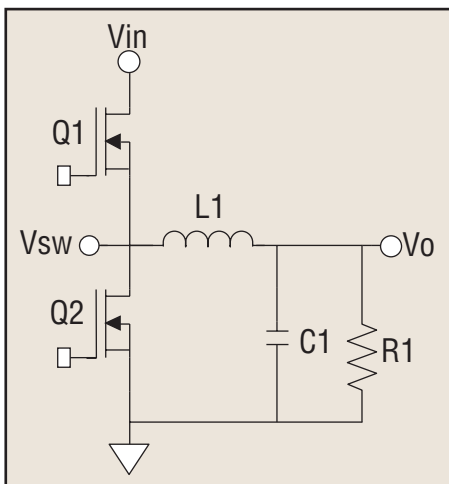
The impediment to bringing the inductor inside the package is its value. Typically, if a power supply is running at frequencies of 500 kHz to 1 MHz, it needs a fairly large inductor. But if you crank up the frequency such that the power stage (controller, gate drive, MOSFETs) can withstand high frequency and still be efficient, then the inductor size can drop. The challenge in raising the frequency is the ability to maintain the efficiency of the overall converter as the frequency goes up. The reward for accomplishing this is a dramatically smaller dc-dc converter.

## Do the Math

The following points offer a first-order empirical derivation of the correlation between the physical size of a buck converter's inductor and its switching frequency.

*Point 1: Size is a function of inductance.*

The inductance value of an inductor is a function of the component's physical parameters:  $N$  = the number of coil turns,  $A$  = the core cross sectional area, and  $l$  = the



**Fig. 1.** Simplified schematic of a typical synchronous buck converter. The inductor current always flows through either Q1 or Q2. During the on-time, Q1 is ON, and inductor current increases. During the off-time, Q2 is ON, and the inductor current decreases. At the on/off transition times, the inductor current has to quickly switch from one FET to the other one.

magnetic path length of the core:

$$L = \mu N^2 A/l$$

Usually, the  $A/l$  value of a core is proportional to its size. The ability to reduce the number of turns  $N$  or the  $A/l$  value depends on reducing the necessary inductance value,  $L$  ( $\mu$  is the permeability constant of the magnetic material).

*Point 2: The inductance required to produce a voltage is inversely proportional to the switching frequency.*

For a given current and voltage, the required inductance value  $L$  is derived from the basic equation:

$$V = L\Delta i / \Delta t \quad (\text{Eq. 1})$$

where  $V$  = output voltage,  $\Delta t$  = off time and  $\Delta i$  = ripple current going through the inductor. The above formula is derived from Faraday's law and assumes that the slope of the inductor current is a constant during the off-time. Solving for the inductor:

$$L = V\Delta t / \Delta i \quad (\text{Eq. 2})$$

Usually, the

ripple current  $\Delta i$  is fixed in a design as a certain percentage of the full-load output current. For a given ripple current and output voltage  $V$ , the focus moves to bringing down the necessary value of  $L$  by reducing the off-time  $\Delta t$  via a shorter switching period. Therefore, a decrease in the MOSFET switching period (increase in the frequency) is the mathematical key to reducing the required induction  $L$ .

*Point 3: MOSFET power dissipation rises with switching frequency.*

The limits to increasing MOSFET switching frequency are found in the physics of the MOSFET semiconductor design.

When a MOSFET is switched off, there is voltage across it, but hardly any current flowing through it. When it is switched on, current is flowing through it, but little voltage is across it, resulting in conduction loss, which is independent of operating frequency. The energy loss in the

MOSFET occurring during on/off and off/on switching transitions is a result of significant current and voltage simultaneously present in the MOSFET. This is called the switching loss, and it occurs twice for every switching period of the converter. For every switching transition, the energy lost  $E_s$  is given by the following expression:

$$E_s = \int_0^{T1} V \cdot Idt \quad (\text{Eq. 3})$$

where  $T1$  is the duration of the on/off or off/on switching transition.

It holds that the more often switching occurs, the more aggregate energy is consumed—switching losses rise as frequency increases.

To simplify the discussion, let us assume the energy lost during the turn-on and turn-off transitions are equal to each other and both transition times are equal to  $T1$ . Therefore, the total switching power loss  $P_s$  is given by:

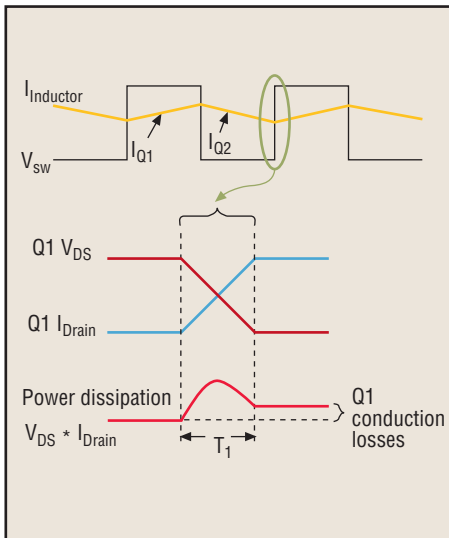


Fig. 2. In the synchronous buck converter, when Q1 is ON the voltage across it is close to zero, and  $V_{sw}$  is high. When Q1 is OFF, the voltage across it is almost  $V_{in}$ , and  $V_{sw}$  is low. During the switching transition region  $T_1$ , the voltage and current changes across Q1 result in the switching power loss.

$$P_s = \frac{2}{T_s} \left( \int_0^{T_1} V \cdot Idt \right) \quad (\text{Eq. 4})$$

where  $1/T_s$  is frequency. This equation demonstrates that for a given  $V$  and  $I$  characteristic during the transition, power dissipation  $P_s$  rises as frequency  $1/T_s$  rises.

**Point 4: Reduced rise/fall time allows higher switching frequencies without incurring unacceptable power loss.**

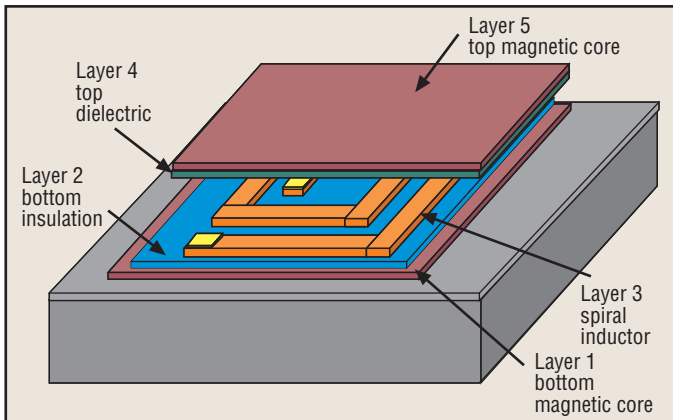
Equation 3 shows the amount of energy consumed during any particular transition (i.e., when the MOSFET turns on or off). As semiconductor design innovations allow shorter, more efficient  $T_1$  times, the power consumed during transition is reduced. Correspondingly, as  $T_1$  falls, frequency can rise without detrimentally increasing power consumption.

By creating MOSFETs with highly efficient  $T_1$  transition times, Enpirion has been able to increase the switching frequency to 5 MHz to 10 MHz, and to drop the required inductance  $L$  by an order of magnitude, allowing the inductor's physical size to be reduced to a size that could be integrated inside the controller package. Another advantage of the higher switching frequency is that the loop bandwidth can be increased, result-

ing in much faster transient response than previous, lower frequency dc-dc converters. Loop bandwidths exceeding 700 kHz have been achieved with this high-frequency design.

To attain the faster transition times, Enpirion used lateral MOSFET technology rather than trench technology. Differences between trench and lateral MOSFETs are mainly in the re-

duced parasitic capacitances, which are traded off for on-resistance. Our design has been optimized for the specific application where high-speed transitions are needed. The optimization process is lengthy and affected by many semiconductor process steps and device design considerations, such as in-line yields at each processing step, and required device reli-



**Fig. 3.** In Enpirion's MEMS-based inductor, a thick electroplated copper spiral coil is sandwiched between two planar magnetic layers.

ability criteria, such as oxide integrity and life.

Trench devices provide excellent cell density at the expense of increased gate charge, whereas lateral devices provide lower gate charge at the expense of cell density. Breakdown voltages are also part of this trade-off since higher breakdown voltages result in lower switching speeds. This effect can be somewhat offset by the design of the channel and drain regions where resistance effects dominate.

While conventional dc-dc converters operate near 250 kHz, and more ambitious devices cycle at around

1 MHz, the approach described here enables switching frequencies in the 5-MHz to 10-MHz range—more than an order of magnitude improvement over the conventional converters. Because of this increase in switching frequency, little inductance is needed and the inductor can be constructed using microelectromechanical system (MEMS) technology.

Enpirion's MEMS-based inductor design consists of a thick electroplated copper (Cu) spiral coil, which is sandwiched between two planar magnetic layers. Enpirion has developed its own proprietary magnetic alloy to meet the technical requirements of high operational speed at high currents.

The inductor fabrication process starts with the bottom magnetic core and its insulation. Then the Cu coil is patterned and electrodeposited as well. Finally, the top magnetic core is deposited on top of a dielectric layer that covers the Cu coil. The inductor fabrication process is a CMOS-compatible process using MEMS-based thick photolithography and electrodeposition techniques.

The resulting inductor can be integrated into a turnkey dc-dc converter package. This co-packaging of inductor and silicon enables circuit designers to drastically reduce board space requirements, while also cutting the development time and bill-of-material costs.

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