



# Application Note

## Paralleling Circuit Design with EN5395/96

### Introduction

The EN5395 and the EN5396 are 9 A voltage-mode synchronous buck converters operating at a fixed frequency of 5 MHz with internal inductors. The EN5395 offers 3-pin VID codes to set the output voltage to one of seven pre-programmed voltages, while the EN5396 offers an adjustable output voltage, set by an external resistor divider. Both devices have a built-in paralleling feature that allows 2 to 4 converters to be paralleled together to increase load current capability up to 36 A. This application note details circuit operation, component selection, performance characteristics and layout considerations to facilitate the design process.

This Applications Note describes the Evaluation board designed specifically to parallel two EN5395/96 devices. However, paralleling can be extended to 4 devices by adding 2 more devices operating in the Slave mode.

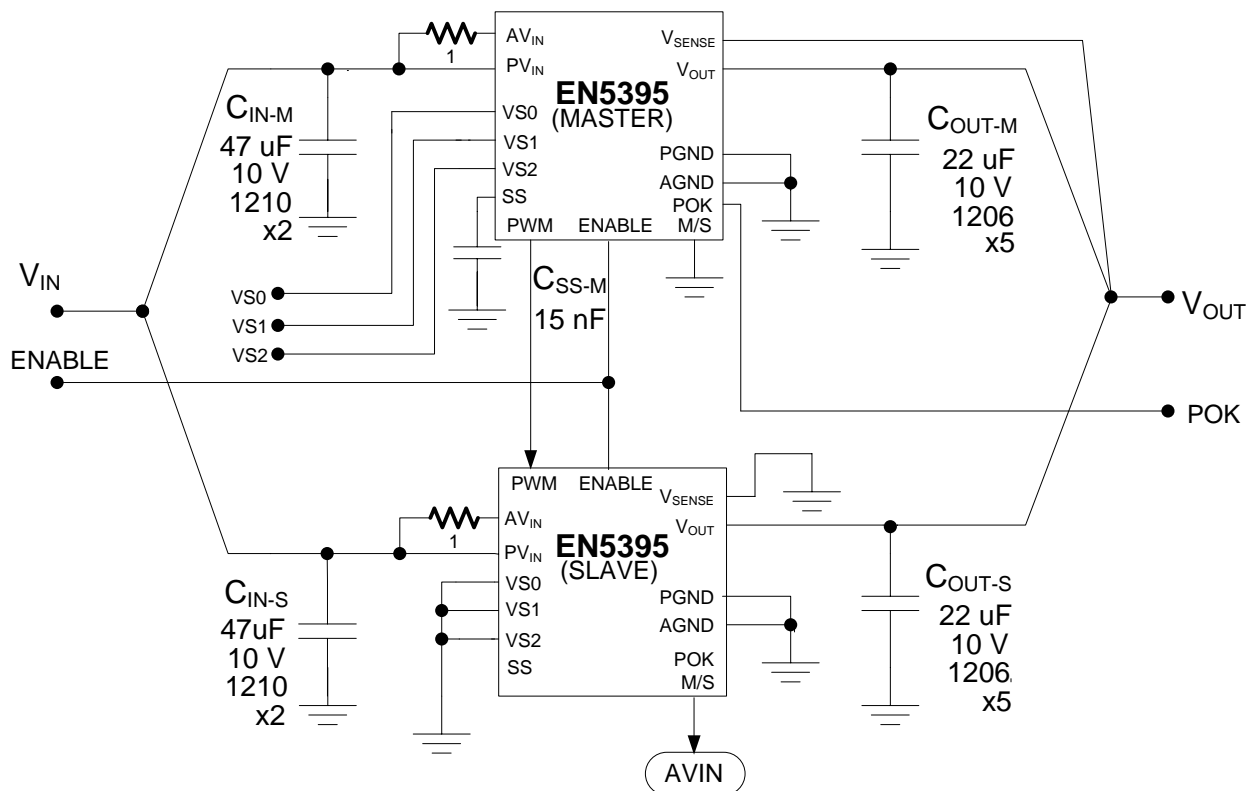


Figure 1. EN5395 Paralleling Circuit



## Component Selection

### Input and Output Capacitors

The power stage for both Master and Slave should be identical. Two 47  $\mu\text{F}$ , 10 V, X5R or X7R ceramic capacitors in 1210 packages are recommended on each converter's input in order to provide sufficient ripple current capability and capacitance on the input. Each converter's output should have five 22  $\mu\text{F}$ , 10 V, X5R or X7R ceramic capacitors in a 1206 package for best ripple.

### Soft-Start Capacitor

A soft-start capacitor on Master is needed to control the soft-start ramp. This capacitor begins to charge when ENABLE and AVIN cross their turn-on thresholds. The typical soft-start time for the output to reach regulation voltage from when  $C_{SS}$  begins to charge is given by:

$$t_{SS} = C_{SS} * 0.075$$

Where the soft-start time  $t_{SS}$  is in ms and the soft-start capacitance  $C_{SS}$  is in nF. Typically, a capacitor around 15 nF is recommended.

### VID Code Setting for EN5395 Paralleling Circuit

Three VID codes VS2, VS1 and VS0 allow the user to obtain one of the 7 pre-programmed output voltages. A logic low can be obtained by pulling the pin low (to ground). A logic high can be obtained by pulling the pin high (to  $V_{IN}$ ). Table 1 shows a matrix of these pre-programmed voltages.

Table 1. Pre-Programmed Output Voltage Setting

VS2	VS1	VS0	Output Voltage
L	L	L	3.3 V
L	L	H	2.5 V
L	H	L	1.8 V
L	H	H	1.5 V
H	L	L	1.25 V
H	L	H	1.2 V
H	H	L	0.8 V

### Resistor Dividers for EN5396 Paralleling Circuit

Resistor dividers are only needed on Master, as stated earlier. Use a 2 k $\Omega$  resistor for the bottom of both dividers. Then the top resistors  $R_{XFB\_M}$  and  $R_{XOV\_M}$  in k $\Omega$  can be calculated by:

$$R_{XFB\_M} = (V_{OUT} - 0.75) / 0.375$$

$$R_{XOV\_M} = (V_{OVTH} - 0.9) / 0.45$$

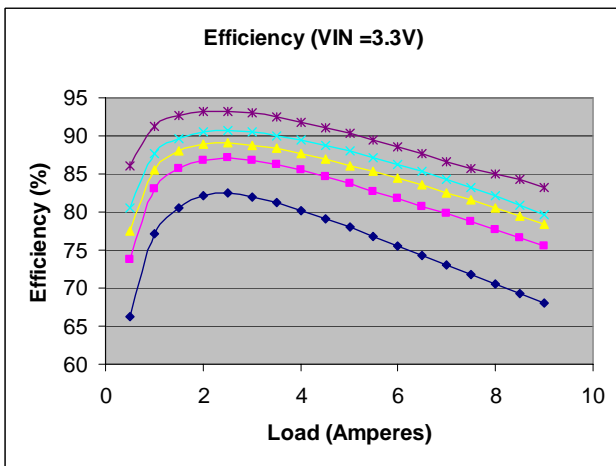


Where  $V_{OUT}$  is the output voltage in V and  $V_{OVTH}$  is the desired over-voltage threshold in V. 1% or better resistors are typically recommended for these resistor dividers.

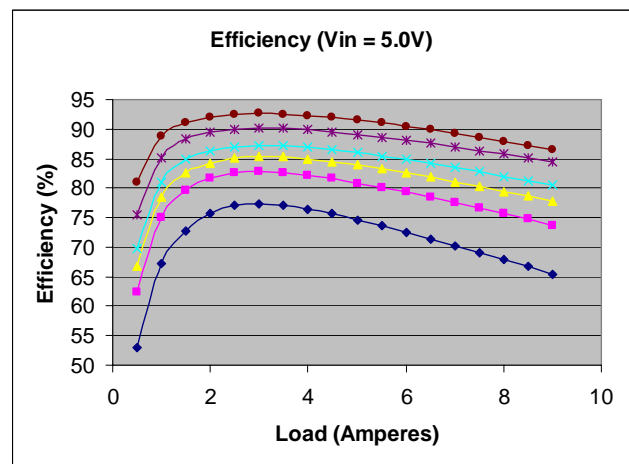
### Typical Performance Characteristics

Circuit of Figure 1,  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$  and  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted.

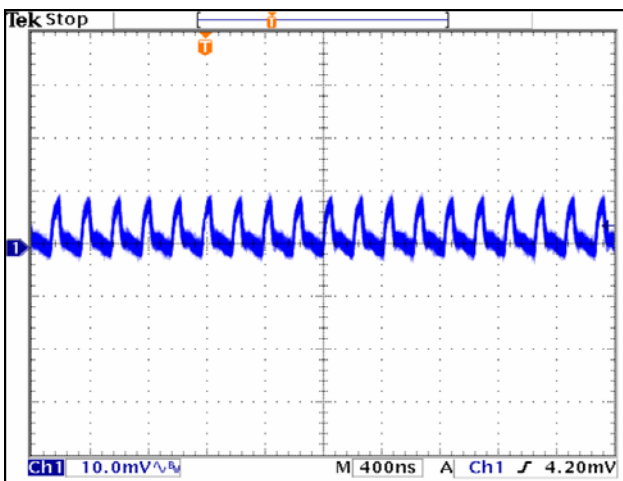
Note: Master/Slave current mismatch ratio is defined as  $(|I_{MASTER} - I_{SLAVE}|) / (0.5 * I_{LOAD}) * 100\%$ .  $X_{XX-M}$  and  $X_{XX-S}$  represent the respective Master and Slave voltage or current.



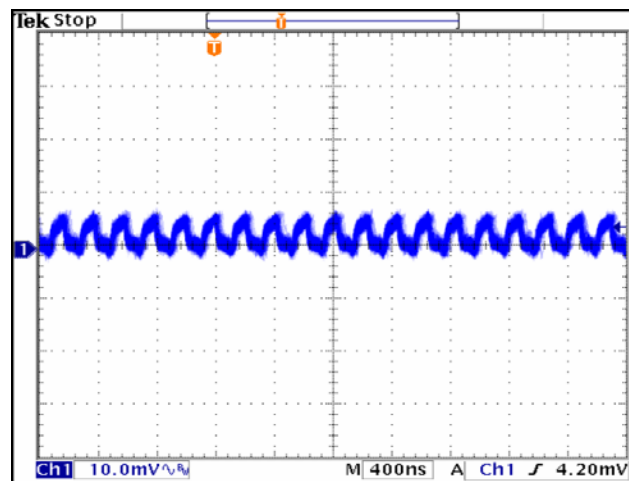
Top to Bottom:  $V_{OUT} = 2.5\text{ V}$ ,  $1.8\text{ V}$ ,  $1.5\text{ V}$ ,  $1.2\text{ V}$ ,  $0.8\text{ V}$



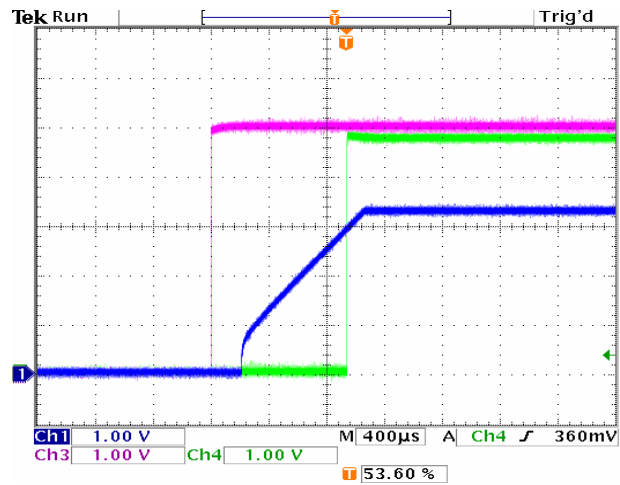
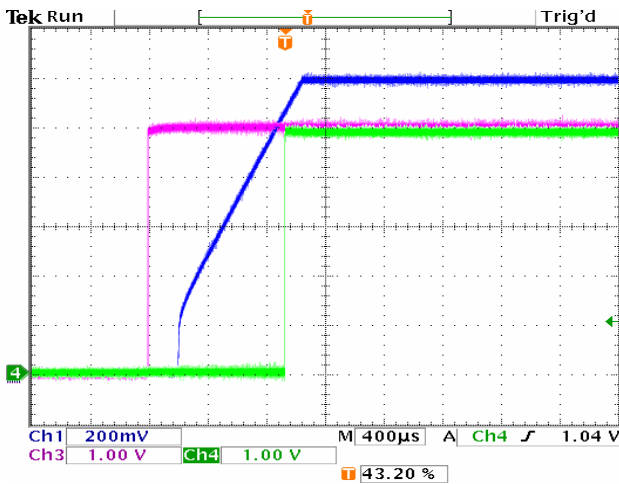
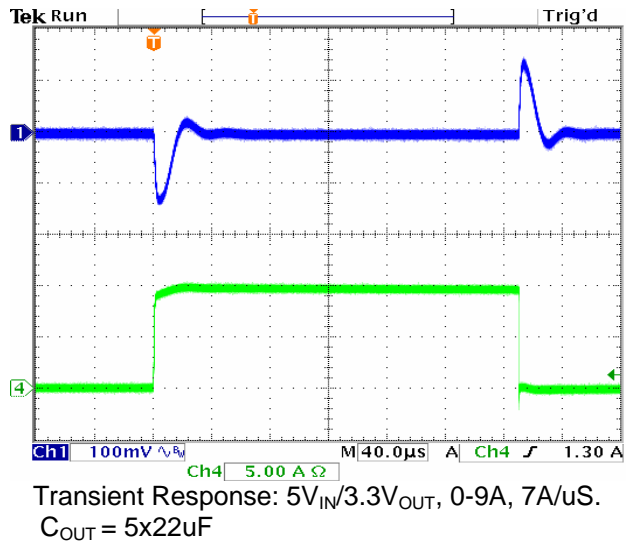
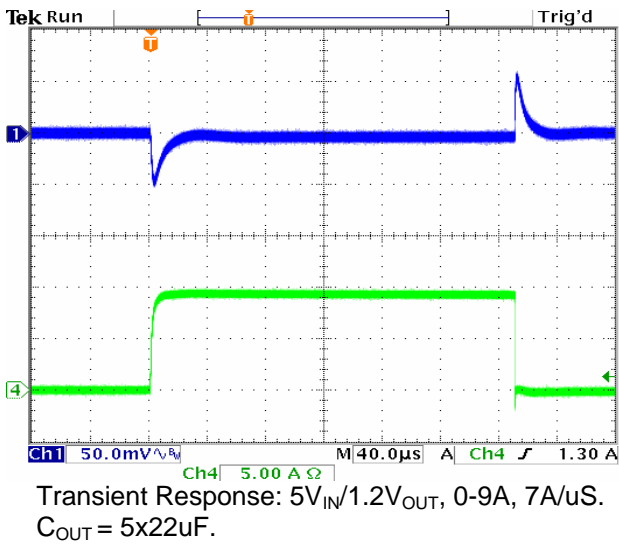
Top to Bottom:  $V_{OUT} = 3.3\text{ V}$ ,  $2.5\text{ V}$ ,  $1.8\text{ V}$ ,  $1.5\text{ V}$ ,  $1.2\text{ V}$ ,  $0.8\text{ V}$



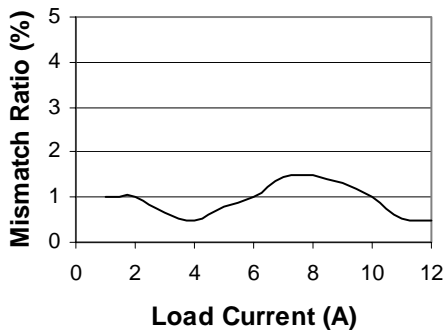
Ripple Voltage,  $5.5V_{IN}/1.2V_{OUT}$ ,  $I_{OUT}=9A$ ,  $C_{OUT} = 5x22\mu F$



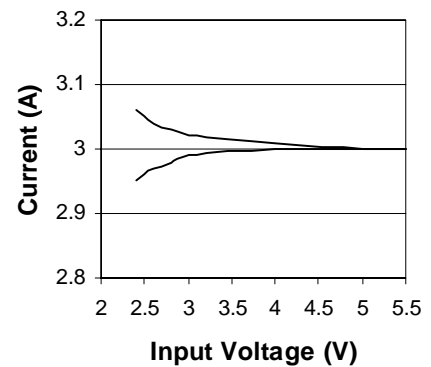
Ripple Voltage,  $3.3V_{IN}/1.2V_{OUT}$ ,  $I_{OUT}=9A$ ,  $C_{OUT} = 5x22\mu F$



**Master/Slave Current Sharing over Load**



**Master/Slave Current Sharing over Line at 6 A Load**



Top: Slave, Bottom: Master



## Layout Considerations

For best current sharing and EMI performance, special attention needs to be paid to layout.

1. Master and Slave should have identical placements with the same values and numbers of input and output capacitors. The power input, input GND, output, and output GND of Master and Slave devices should be connected together via short PCB traces of identical width and length before connected to the system input and output. The output and output GND connection is especially critical and will affect current sharing to a great extent. The maximum resistance difference in PCB traces between the outputs should be less than 10 m $\Omega$ . The maximum difference of the input voltage between any two devices should be less than 50 mV. If the paralleling point cannot be equidistant from all converters, the one closest to the paralleling point should be Master.
2. All Master and Slave devices should have their ENABLE pins tied together and should be operated simultaneously with a fast rising edge of 10  $\mu$ s or less, to ensure that devices start up at the same time. Startup imbalance could lead to OCP condition in the first device to start up.
3. The PWM pin from the Master device is connected to all Slave device PWM pins. Use short and wide traces to make connections and avoid routing these traces around noisy nodes in the circuit.
4. Master VSENSE pin should be connected to the output for voltage regulation. The VSENSE pin is typically connected to the paralleling point at the output.
5. Each individual converter layout should follow the layout guidelines stated in the EN5395 and EN5396 datasheets.

## Conclusions

Both the EN5395 and EN5396 work well in paralleling circuits to deliver greater load current. Current sharing is excellent, typically within 2 %. Stable operation with internal compensation and minimal component count offers compact solutions for higher current applications.

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