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EP53XXXUI QFN Package Soldering Guidelines

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1.0 INTRODUCTION

Enpirion's EP53XXXUI power converter packages are designed with a plastic leadframe package technology that utilizes copper leadframes and mold caps with System in Package (SiP) construction to form a Quad Flat No-lead (QFN) package. QFN package technology is ideal for power conversion devices due to the solderable exposed bottom copper leadframe for thermal dissipation and the resulting low package thermal resistance, the smaller package footprint and thickness, large lead size and pitch, and excellent lead co-planarity. The EP53XXXUI Package Outline Drawing is shown in Figure 1 with the overall package dimensions and details of the solderable leads.

In order to ensure a high performance and reliable solder connection of the EP53XXXUI QFN package to a PCB, this document provides recommendation guidelines for PCB design and solder assembly of the EP53XXXUI package.

2.0 PCB DESIGN RECOMMENDATIONS

The EP53XXXUI power converter package requires a high quality solder connection to a PCB for optimum electrical and thermal package performance. Recommendations for the design and layout of the PCB for soldering the EP53XXXUI QFN package are presented to obtain optimum package performance.

2.1 Pad Layout

Figure 2 shows the PCB pad layout for the EP53XXXUI QFN package. The dashed line represents the outline of the EP53XXXUI package body after solder attach to the PCB. There are 16 perimeter leads that must be soldered for proper function of the EP53XXXUI power converter package. See the EP53XXXUI Datasheet for names and interconnection of the package leads.

Recommendation: The PCB layout should NOT have any traces or other top layer metal routed under the EP53XXXUI package body outline. All traces should extend outside the EP53XXXUI package body.

Recommendation: The PCB layout should include a top layer solder mask that fully covers the non-solderable area under the EP53XXXUI package body outline.

The EP53XXXUI QFN package design uses a non-pullback lead design where the leads extend completely to the edges of the package and are exposed on the sides of the package (see the Package Outline Drawing in Figure 1). This non-pullback lead design allows for filleting of the solder on each lead resulting in a robust and reliable solder joint.

Recommendation: The PCB layout should provide pad lengths that extend beyond the package body by at least 0.20mm (8 mil) to provide solder filleting on the leads for improved solder joint reliability, inspection, and lead probing and to allow for better package placement tolerances.

2.2. Pad Design

2.2.1 Solder Mask Pad Definition

In PCB design, the surface mount solder pads can be defined as either Solder Mask Defined (SMD) or Non-Solder Mask Defined (NSMD). The difference between these two solder mask pad definitions is in the proximity of the solder mask to the metal pad. In SMD pads the solder mask opening is smaller than the metal pad and overlaps the metal on all sides. The solder mask opening defines the solderable area of the pad. In NSMD pads the solder mask opening is larger than the metal pad and does not overlap the metal. The metal edge defines the solderable area of the pad. Figure 3 shows the details of SMD and NSMD pads.

Since the metal etching process in PCB manufacture has significantly tighter alignment and etch tolerances than the alignment registration of the solder masking process, which is typically ±0.075 mm (3 mil), a more accurate solder pad land pattern can be obtained with NSMD pads. Likewise, with SMD pads, the solder mask that overlaps the metal pad introduces additional height above the metal surface that may affect solder joint adhesion and reliability.

Recommendation: The PCB layout should use NSMD pad definitions for all leads and pads for the EP53XXXUI QFN package. The solder mask opening must be defined at least 0.075 mm (3 mil) larger than the metal pad on all sides.

2.2.2 Solder Pad Land Pattern

The EP53XXXUI QFN package has symmetric solder pads around the perimeter of the package for signals. (See the EP53XXXUI Package Outline Drawing in Figure 1).

Recommendation: The PCB layout should conform exactly to the power converter QFN package pads as defined in Figure 2. The 0.20 mm (8 mil) extended pad length defined in Section 2.1 should be applied. This will provide the highest solder joint reliability between the EP53XXXUI QFN package and the PCB.

Design variation in the PCB pad layout is allowed for any optional probe pads adjacent to signal pads that extend outside the EP53XXXUI QFN package footprint.

Recommendation: The PCB layout may include probe pads that should be designed with a small trace from the signal pad connecting the probe pads as shown in Figure 4. This trace must be at least 0.20 mm (8 mil) long and covered with solder mask to prevent solder from flowing onto the probe pad.

2.3 Pad Plating

A uniform metal plating thickness on the PCB will ensure reliable, high yield EP53XXXUI QFN package solder assembly yield.

Recommendation: The following plating guidelines for various PCB metal plating processes should be used:

- For an Electroless, Nickel-Immersion, Gold (Au) finish (ENIG), to prevent solder joint embrittlement, the thickness of the Au must be between 0.05 μm to 0.20 μm.
- A PCB with an Organic Solderabillity Preservative (OSP) coating is recommended as an alternative to an ENIG plating
- For a PCB with a Hot Air Solder Leveling (HASL) finish, the surface finish should be maintained within a 28μm range.

3.0 SOLDERING AND REFLOW

3.1 Solder Paste Deposition

A stencil-printing process will be required for deposition of solder paste to the PCB for reflow of the EP53XXXUI QFN package to the PCB. The stencil-printing process requires the use of an aperture based metal stencil where solder is transferred through the apertures onto the solder pads of the PCB. To minimize solder voids and ensure maximum electrical and thermal connectivity of the EP53XXXUI package to the PCB, large pads, solder volume, and solder leaching must be considered in the stencil design. The design and fabrication of the stencil determines the quality of the solder paste deposition onto the PCB and the resulting solder joint after reflow. The primary stencil parameters are aperture size, thickness, and fabrication method.

3.1.1 Solder Stencil

Figure 5 shows the solder stencil aperture layout for the EP53XXXUI QFN package.

Recommendation: The stencil aperture openings for all leads should have a 1:1 size ratio with the leads of the EP53XXXUI QFN package.

Recommendation: The stencil should be made from stainless steel and have a thickness between 0.102 (4mil) and 0.127μm (5mil).

Recommendation: The stencil should be fabricated by chemical etching with electropolishing or by laser cutting. A tapered wall (up to 5°) on the apertures will facilitate solder paste release when the stencil is lifted from the PCB.

3.1.2 Solder Paste
Various types and grades of solder paste can be used for surface mounting the power converter QFN package. For leaded applications, a Sn-Pb solder can be used and for leadfree application a Sn-Ag (SA) or Sn-Ag-Cu (SAC) solder can be used.

Recommendation: Any Type 3 solder paste that is either water-soluble or no clean is acceptable.

3.2 Package Placement
The EP53XXXUI QFN package is placeable onto the PCB using industry standard component pick-and-place systems that have a placement accuracy of ±0.05mm (±2 mil).

Recommendation: For higher placement accuracy a component pick-and-place system with a top-and-bottom vision system should be used.

Recommendation: The EP53XXXUI QFN package should be released between 25—50µm (1—2 mil) into the solder paste.

3.3 Solder Reflow
The EP53XXXUI QFN package may be surface mount soldered using standard IR or IR convection SMT reflow process. The EP53XXXUI QFN package is qualified for a maximum of three (3) reflow cycles at 260°C peak reflow temperature according to the IPC/JEDEC J-STD-020C standard.

Recommendation: When using a solder paste with a no-clean flux a Ni (nitrogen) purge should be used during reflow.

The thermal reflow profile for component placement onto a PCB and the actual temperature of the component is dependent on various factors including: PCB thickness; PCB Cu (copper) weight; component density; component location; and size and thermal mass of other surrounding components. When using an IR reflow oven the location of other larger components can cause shadowing onto a specific component.

Recommendation: The thermal reflow profile for the EP53XXXUI QFN package should be determined for each specific location on the PCB.

3.3.1 Solder Reflow Profile
Typical solder reflow profiles for both leaded and leadfree solders are shown in Figures 6 and 7, respectively.

Table 1 Recommended Solder Reflow Profile Parameters for Leaded Solder

Leaded Solder	**Reflow Parameters**		
Reflow Profile Segment	Min	Recommended	Max
Preheat Temperature (°C)	100	140	150
Preheat Time (sec)	60	110	120
Ramp Up Rate (°C/sec)	1.5	2	3
Dwell Time above 183°C (sec)	50	75	85
Peak Temperature (°C)		215	240
Dwell Time at Peak (sec)	1	5	10
Ramp Down (°C/sec)	3	4	6

Table 2 Recommended Solder Reflow Profile Parameters for Lead-Free Solder

Lead-Free Solder	**Reflow Parameters**		
Reflow Profile Segment	Min	Recommended	Max
Preheat Temperature (°C)	150	175	200
Preheat Time (sec)	60	130	180
Ramp Up Rate (°C/sec)	2	3	4
Dwell Time above 217°C (sec)	60	90	120
Peak Temperature (°C)		250	265
Dwell Time at Peak (sec)	10	12	20
Ramp Down (°C/sec)	3	4	4

3.3 Solder Joint Inspection

An inspection of the solder joint between the solder pads of the EP53XXXUI QFN package and the PCB should be performed.

Recommendation: Sample inspection monitoring at regular intervals during solder reflow should be performed of the solder joint between the solder pads of the EP53XXXUI QFN package and the PCB.

The best visual inspection tool for inspection of the EP53XXXUI QFN package solder joint on the PCB is a transmission X-ray, which can identify defects such as solder bridging, shorts, opens, and large voids (Note: small voids in large solder joints are not detrimental to the reliability of the solder joint). An additional visual inspection tool consists of side view inspection, such as 90° mirror projection, to determine component flatness and solder joint volume.

Recommendation: If possible, both transmission X-ray and a side view inspection process should be performed for visual solder joint inspection.

5.0 SUMMARY

This paper presents recommendations for PCB design and process procedures for use with the Enpirion EP53XXXUI QFN power converter packages. Proper and recommended design principles for PCB land pattern design and construction are presented. A detailed process description and recommendations for soldering and reflow including solder stencil printing, PCB preheating and localized heating, solder reflow, and QFN package placement are presented.

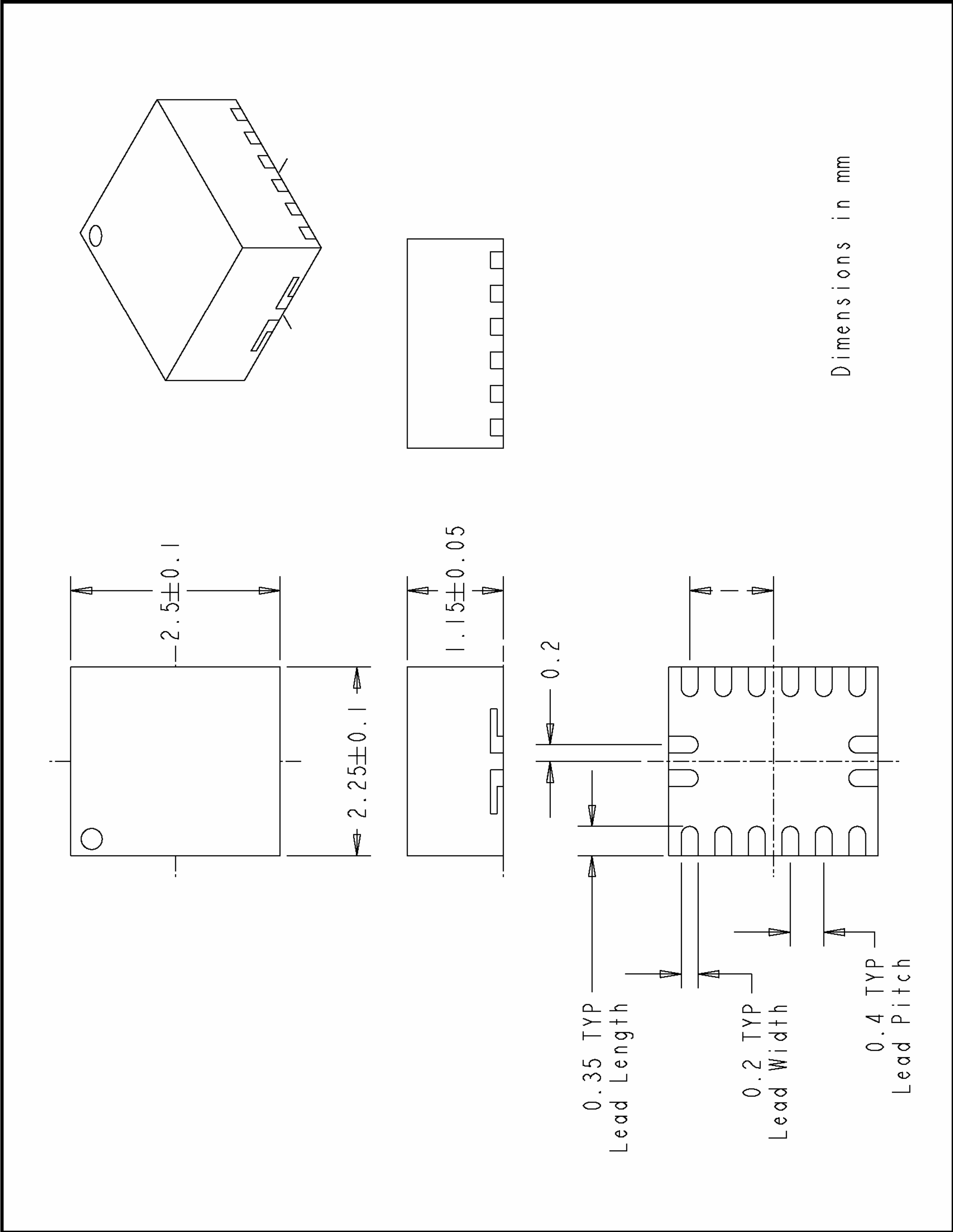

Figure 1: EP53XXXUI Package Outline Drawing

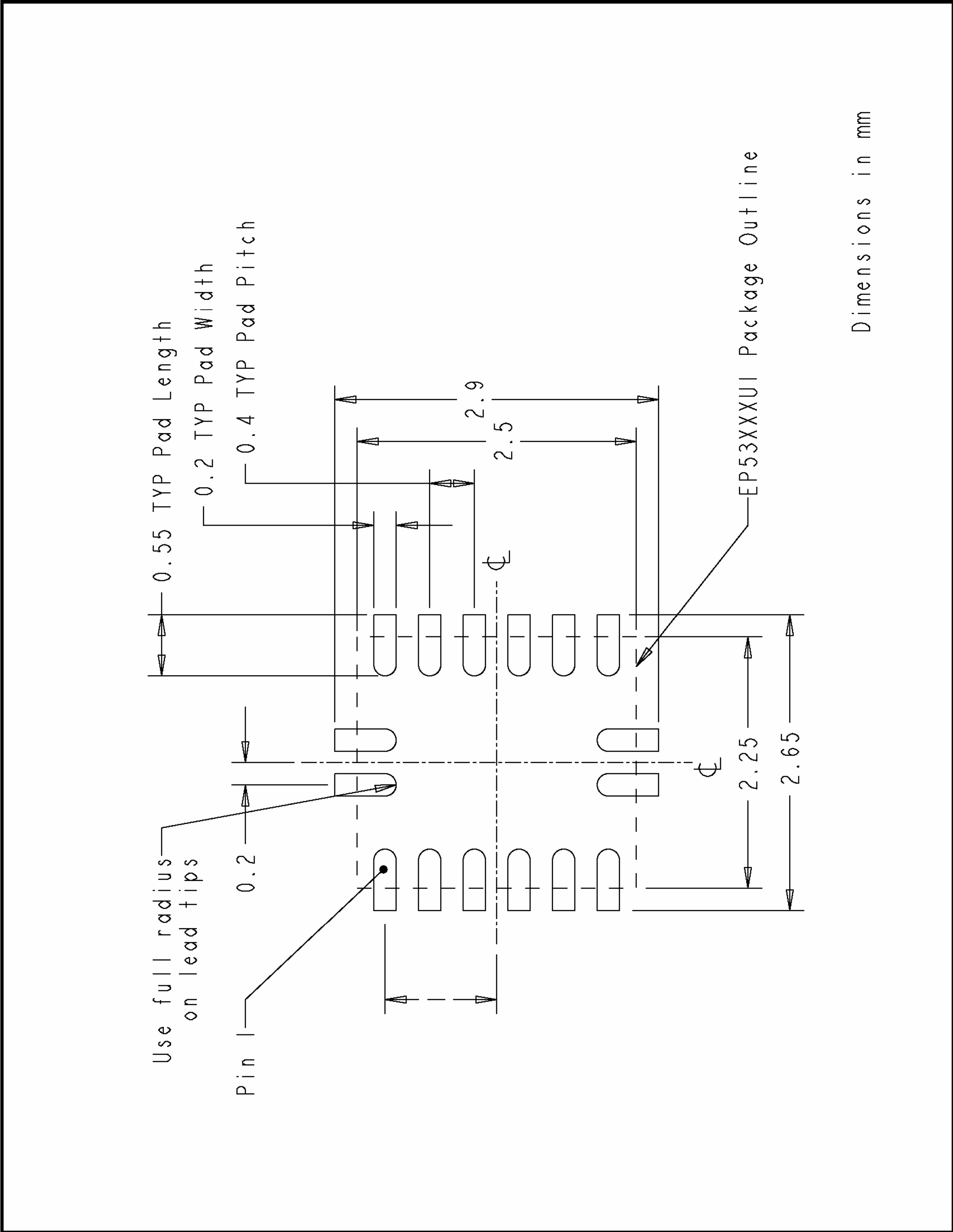

Figure 2 PCB Land Pattern for soldering EP53XXXUI QFN package

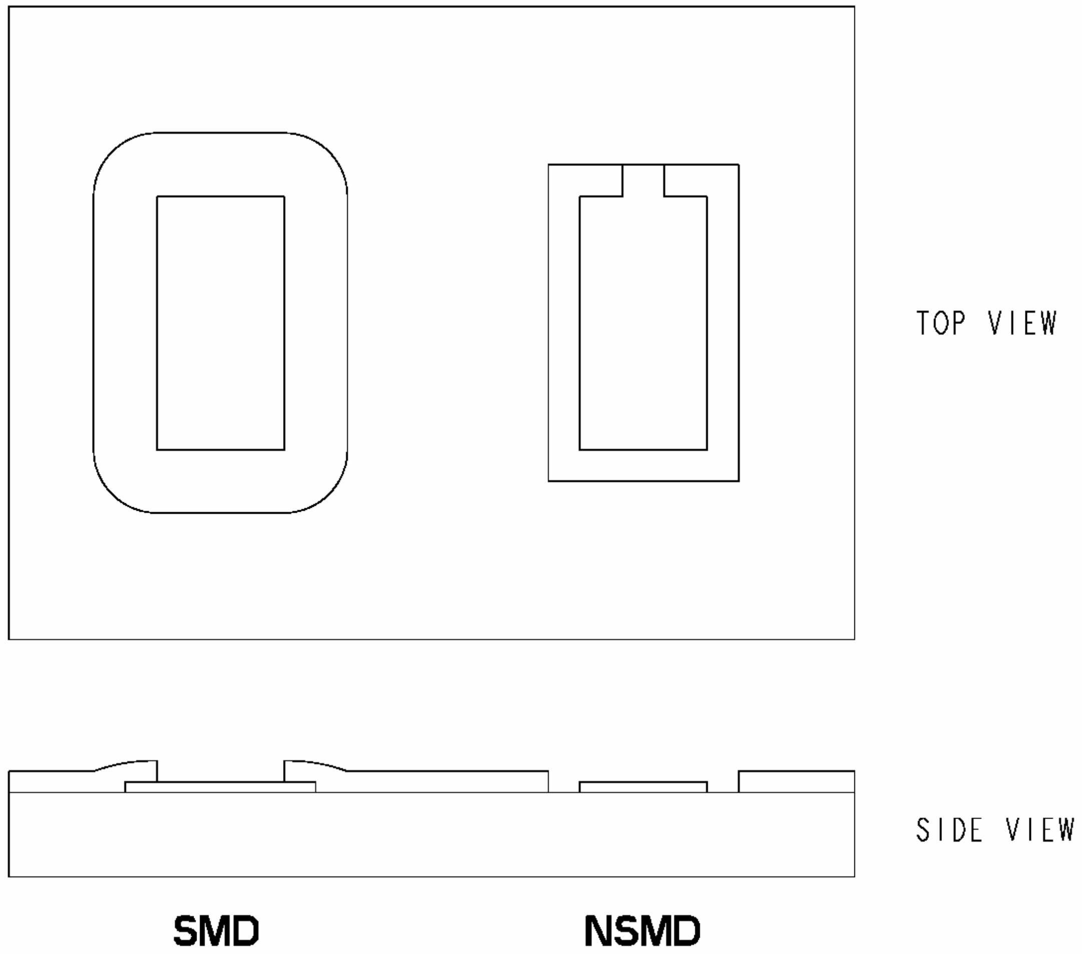

Figure 3: PCB Pad SMD and NSMD definitions

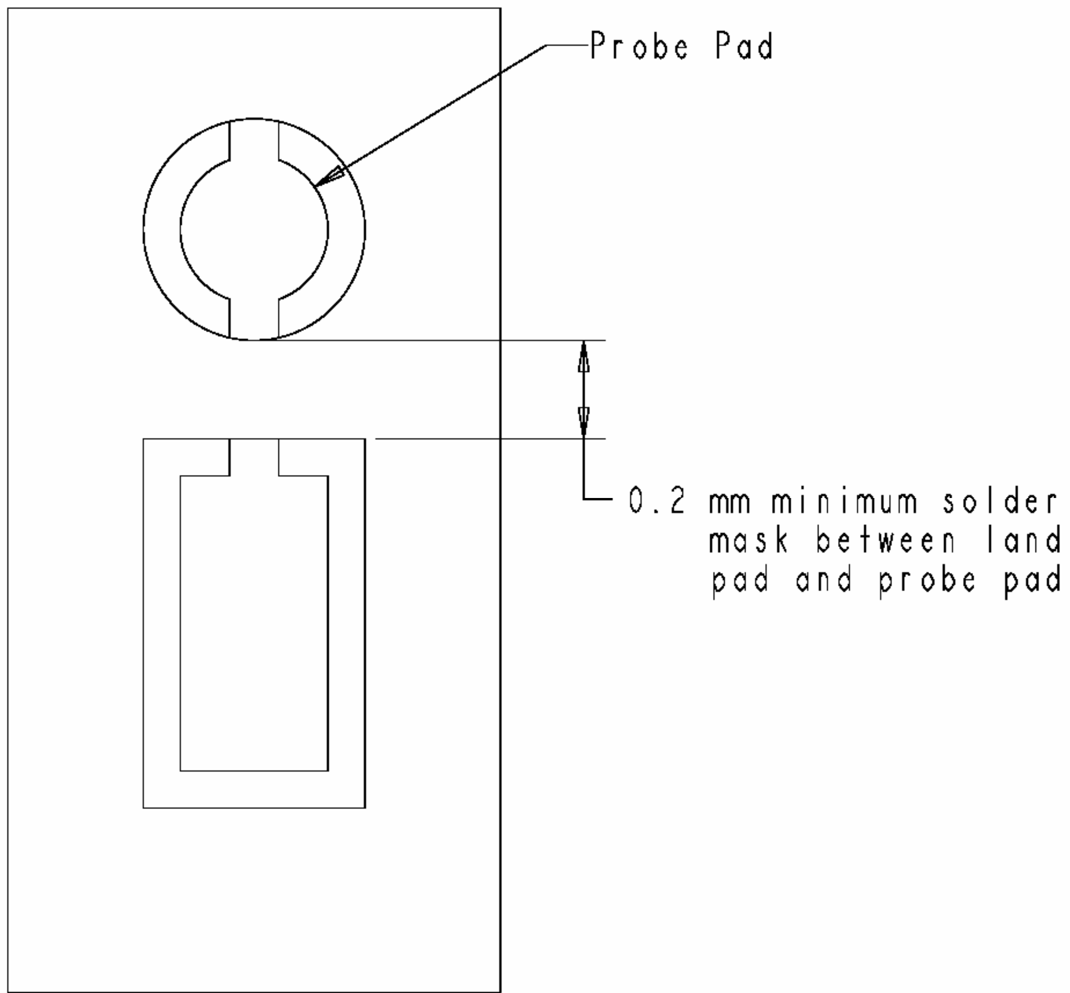

Figure 4: PCB pad design for probe pads

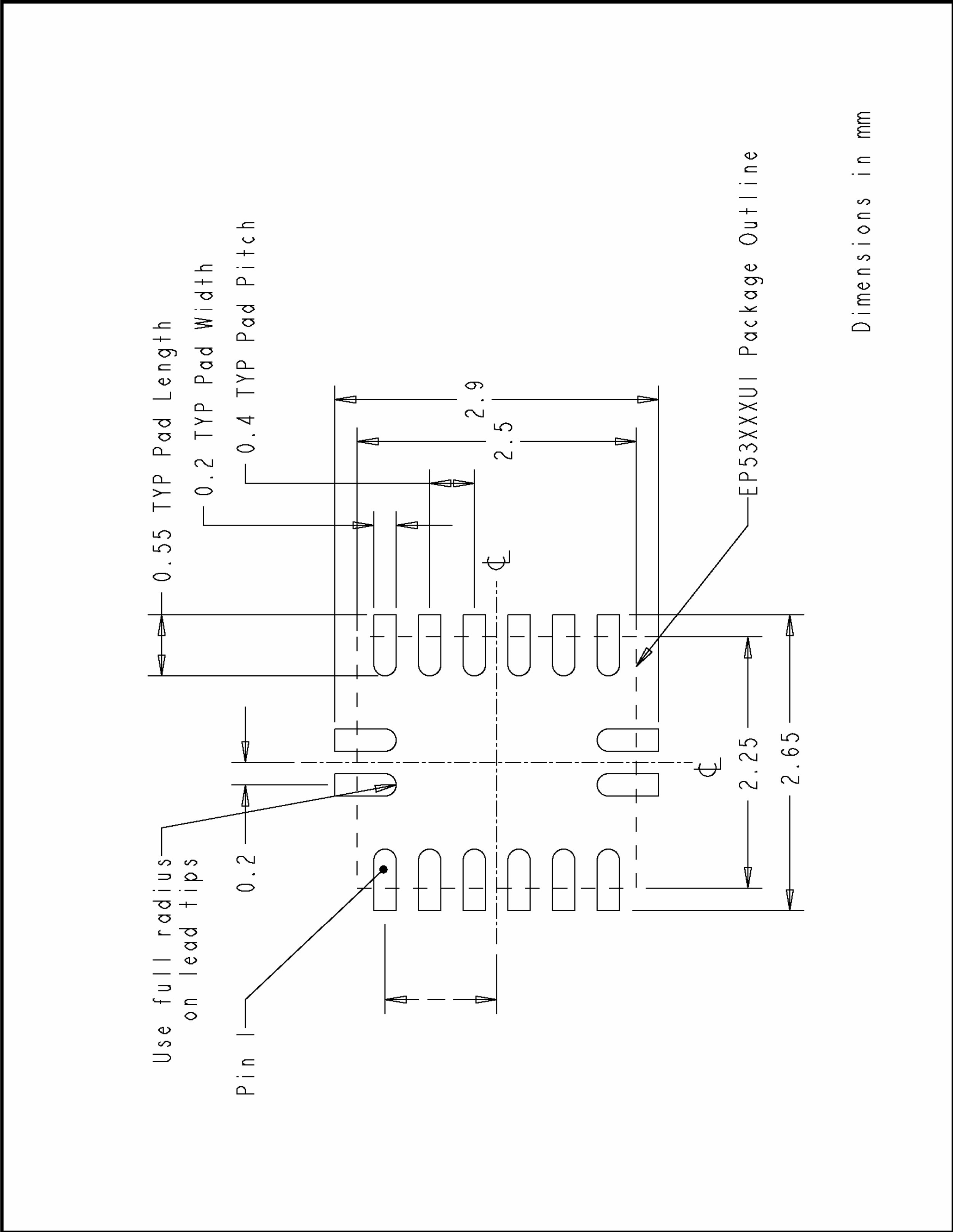

Figure 5 Solder stencil aperture layout for the EP53XXXUI QFN package

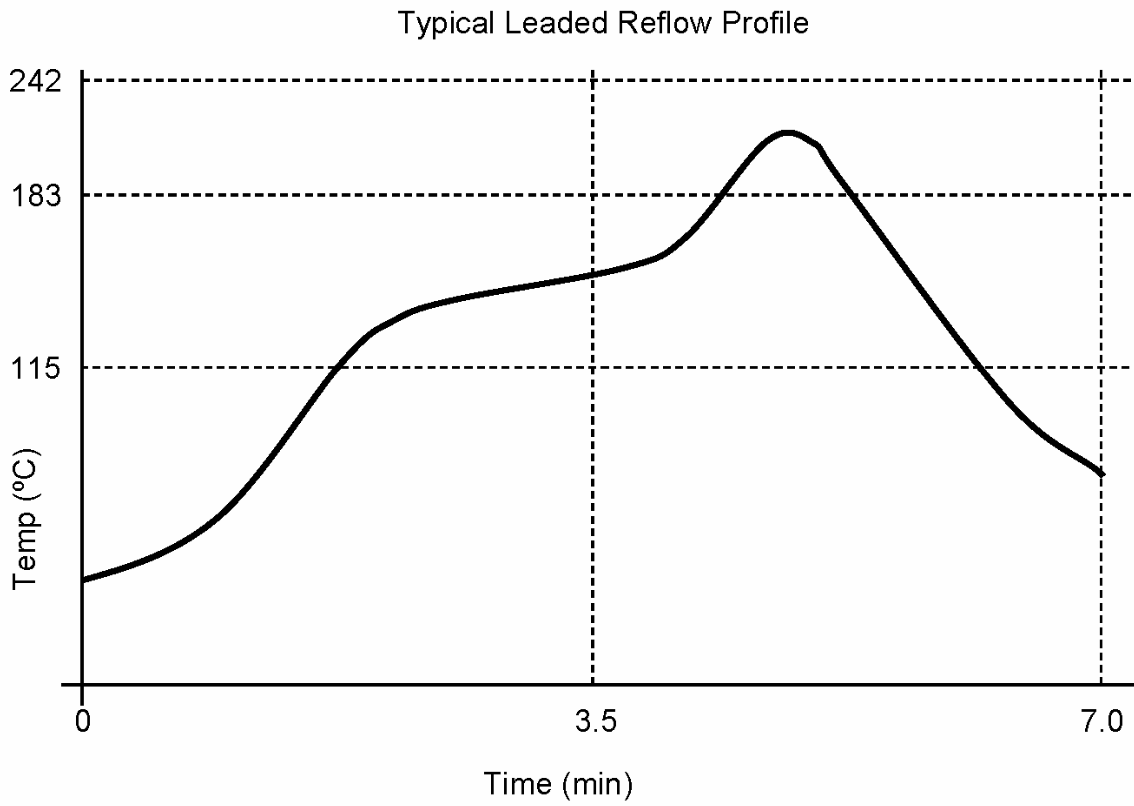

Figure 6: Typical Leaded Reflow Profile

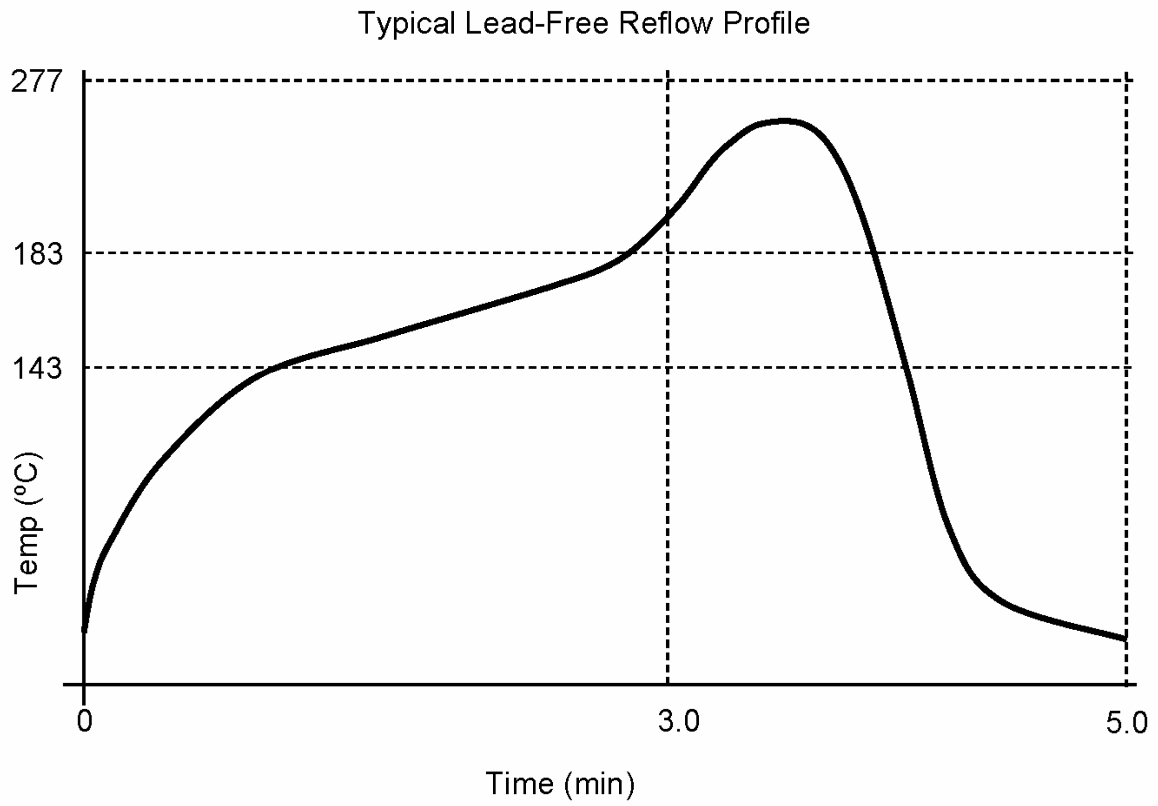

Figure 7: Typical Lead-Free Reflow Profile